

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
A	0000891242	PRODUCTION RELEASED	2010-04-13

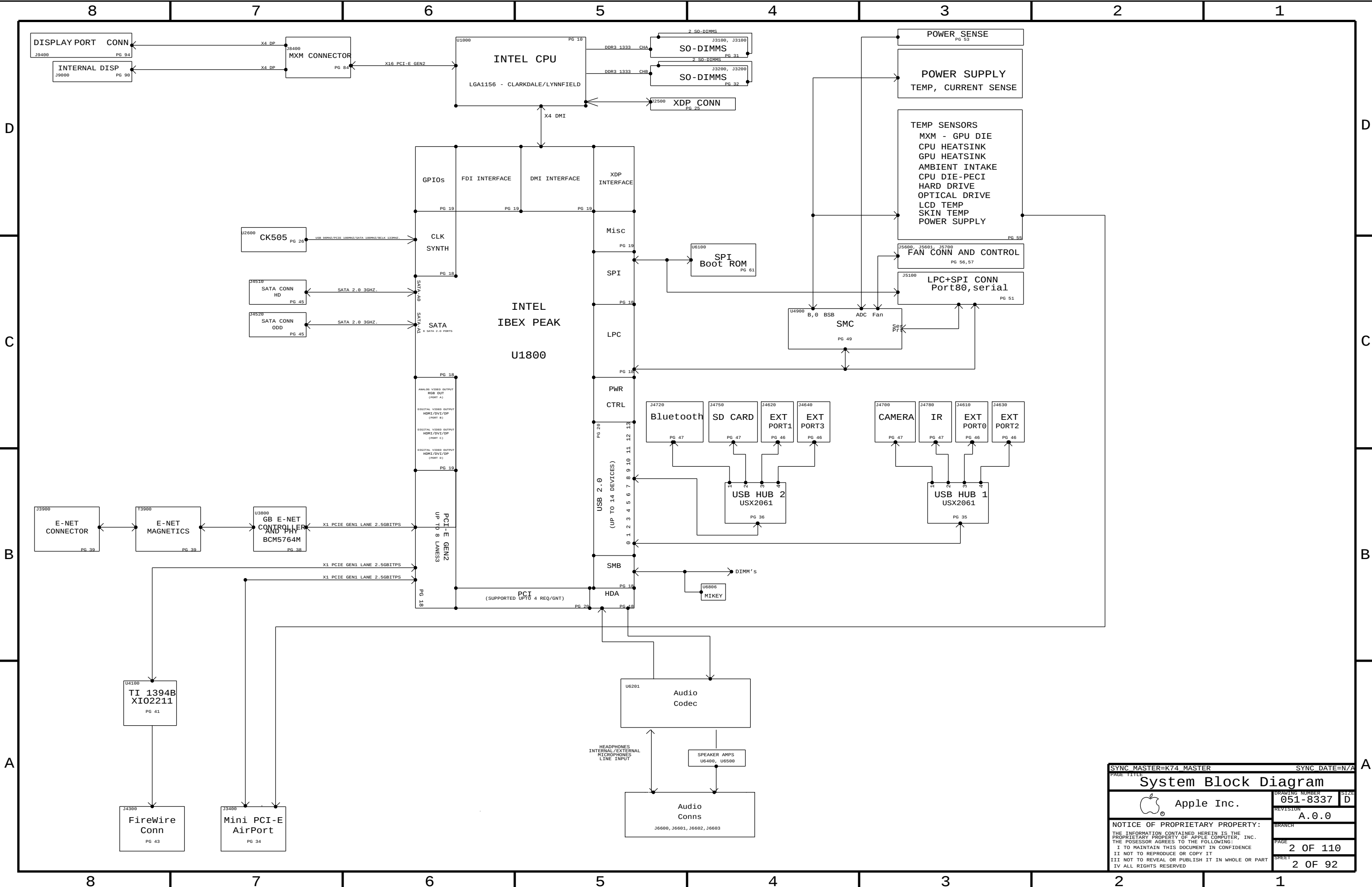
SCHEMATIC, MLB, "OLVIA"

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1	Table of Contents	K74_MASTER	N/A
2	System Block Diagram	K74_MASTER	N/A
3	Power Block Diagram	K74_MASTER	N/A
4	BOM Configuration	K74_MASTER	N/A
5	Power Conn / Alias	K74_MASTER	N/A
6	Holes	K74_MASTER	N/A
7	UNUSED SIGNAL ALIAS	K74_MASTER	N/A
8	Signal Aliases	K74_MASTER	N/A
9	CPU DMI/PEG/FDI/RSVD	K74_MASTER	N/A
10	CPU CLOCK/MISC/JTAG	K74_MASTER	N/A
11	CPU DDR3 INTERFACES	K74_MASTER	N/A
12	CPU POWER	K74_MASTER	N/A
13	CPU GROUNDS	K74_MASTER	N/A
14	STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU	NICK	12/08/2009
15	CPU NON-GFX DECOUPLING	NICK	12/08/2009
16	CPU/PCH GFX DECOUPLING	K74_MASTER	N/A
17	PCH SATA/PCIE/CLK/LPC/SPI	NICK	12/08/2009
18	PCH DMI/FDI/GRAPHICS	K74_MASTER	N/A
19	PCH PCI/FLASHCACHE/USB	NICK	12/08/2009
20	PCH MISC	K23F	11/30/2009
21	PCH POWER	K23F	11/30/2009
22	PCH GROUNDS	K23F	11/30/2009
23	PCH DECOUPLING	K74_MASTER	N/A
24	EXTENDED DEBUG PORT(XDP)	NICK	12/08/2009
25	CLOCK (CK505)	K23F	11/30/2009
26	DDR3 RESET	MATT	01/06/2010
27	CHIPSET SUPPORT	K74_MASTER	N/A
28	DDR3 Vref Margining	MATT	01/06/2010
29	MEMORY CAPS	K74_MASTER	N/A
30	DDR3 SO-DIMMs 0 & 2	K74_MASTER	N/A
31	DDR3 SO-DIMM CONNECTOR B	K74_MASTER	N/A
32	DDR3 ALIAS AND BITSWAPS	K74_MASTER	N/A
33	PCI-E MiniCard Connector	K74_MASTER	N/A
34	USB HUB 1	K74_MASTER	N/A
35	USB HUB 2	K74_MASTER	N/A
36	Caesar II/IV Support	MASTER	N/A
37	Ethernet PHY (Caesar II/IV)	T27	11/30/2009
38	Ethernet Connector	MASTER	N/A
39	FireWire LLC/PHY (XI02213B)	MASTER	N/A
40	FW: 1394B MISC	MASTER	N/A
41	FIREWIRE CONNECTOR	MASTER	11/17/2009
42	SATA Connectors	K74_MASTER	N/A
43	EXTERNAL USB CONNECTORS	MASTER	11/30/2009
44	Internal USB Connections	MASTER	11/06/2009
45	SD READER CONNECTOR	K74_MASTER	N/A
46	SMC	K74_MASTER	N/A
47	SMC Support	K74_MASTER	N/A
48	LPC+SPI Debug Connector	K23F	11/30/2009

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50	CPU/GPU POWER SENSE	K74_MASTER	N/A
51	HDD TEMP SENSE	K74_MASTER	N/A
52	REMOTE TEMP/POWER SENSORS	NICK	11/06/2009
53	HD AND OD FAN	K74_MASTER	N/A
54	CPU FAN & AMBIENT SENSE	K74_MASTER	N/A
55	SPI ROM	K23F	11/30/2009
56	AUDIO: CODEC/REGULATOR	BREECE	02/02/2010
57	AUDIO: FILTER/BUFFER	BREECE	02/02/2010
58	AUDIO: SPEAKER AMP_1	BREECE	02/02/2010
59	AUDIO: SPEAKER AMP	BREECE	02/02/2010
60	Audio: MLB to I/O Conn.	BREECE	02/02/2010
61	AUDIO: Detects/Grounding	BREECE	02/02/2010
62	AUDIO: Mikey	BREECE	02/02/2010
63	POWER SEQUENCING ENABLES	K74_MASTER	N/A
64	POWER SEQUENCING PGOOD	K74_MASTER	N/A
65	VREG: PPVCORE_S0_CPU	K74_MASTER	N/A
66	VREG: CPU CORE - PHASES 1-3	K74_MASTER	N/A
67	VREG: CPU CORE - CAPS	K74_MASTER	N/A
68	CPU VTT REGULATOR	NICK	12/08/2009
69	IBEX PEAK CORE	K74_MASTER	N/A
70	5V_S3 / 3V3_S5 VREGS	NICK	12/08/2009
71	1.5V / 1.8V VREGS	K23F	11/30/2009
72	3.42 G3HOT SUPPLY	K74_MASTER	N/A
73	S3+S0 FETS	K74_MASTER	N/A
74	MXM PCIe, DP & Power	K23F	11/30/2009
75	MXM I/O	K74_MASTER	N/A
76	MXM PCIe CAPS	K23F	11/30/2009
77	Display: Aliases	K74_MASTER	N/A
78	Display: Int DP Connector	K74_MASTER	N/A
79	DISPLAY: DP REDRIVER	DAVE	01/07/2010
80	DISPLAYPORT CONNECTIONS	DAVE	01/07/2010
81	Display: Ext DP Connector	K74_MASTER	N/A
82	K74/K75 RULE DEFINITIONS	K74_MASTER	N/A
83	Memory Constraints	K74_MASTER	N/A
84	PCIe/DMI/FDI/SATA CONSTRAINTS	K74_MASTER	N/A
85	IBEX PEAK CONSTRAINTS	K74_MASTER	N/A
86	ENET/SD/FW/AUD CONSTRAINTS	K74_MASTER	N/A
87	GRAPHICS CONSTRAINTS	DAVE	01/07/2010
88	SMC Constraints	TEMP	12/09/2009
89	POWER CONSTRAINTS	K74_MASTER	N/A
90	PM RESETS ENABLES PGOOD CONST	K74_MASTER	N/A
91	K74/K75 ICT/FCT	K74_MASTER	N/A

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DRAWING TITLE		DRAWING NUMBER		SIZE
SCHEMATIC, "OLVIA", MLB		051-8337		D
 Apple Inc.		REVISION		
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-1107	PCBA, MLB, DEV, K74	DEVELOPMENT, DEV_GROUP
639-0698	PCBA, MLB, K74, 2.93GHZ, CKD	K74, 2P93GHZ_CKD_CPU, BASIC, CLARKDALE_73W
639-0707	PCBA, MLB, K74, 3.06GHZ, CKD	K74, 3P06GHZ_CKD_CPU, BASIC, CLARKDALE_73W
639-0808	PCBA, MLB, K74, 3.29GHZ, CKD	K74, 3P29GHZ_CKD_CPU, BASIC, CLARKDALE_73W
639-0695	PCBA, MLB, K74, 3.46GHZ, CKD	K74, 3P46GHZ_CKD_CPU, BASIC, CLARKDALE_73W
639-0991	PCBA, MLB, K74, 3.60GHZ, CKD	K74, 3P60GHZ_CKD_CPU, BASIC, CLARKDALE_73W
639-0694	PCBA, MLB, K74, 2.53GHZ, LFD	K74, 2P53GHZ_LFD_CPU, BASIC, LYNNFIELD_82W

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE, XDP, MXM, XDP_CPU_BPM, PCH_VRM, BUF_CLK, HUB_USX2061, FW_TI_INT_VREG, BCM5764M, SD_USB, METAL_IO, PRODUCTION
DEV_GROUP	XDP_CONN, LPCPLUS, M0J0MUX, CPU_1V5_SENSE, VREFMRGN

CPU SOCKET & ILM SUB-BOMS

ALTERNATE SOCKET VENDORS MUST USE MATCHING ILM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0963	1	SOCKET, LGA1156, CPU-LF	U1000	CRITICAL	MOLEX_SOCKET
604-1161	1	ASSY, PURCHASED, ILM, MOLEX, K74	ILM	CRITICAL	MOLEX_SOCKET
511S0969	1	SOCKET, LGA1156, CPU-LF	U1000	CRITICAL	FOXCONN_SOCKET
604-1246	1	ASSY, PURCHASED, ILM, MOLEX, K74	ILM	CRITICAL	FOXCONN_SOCKET

BOM NUMBER	BOM NAME	BOM OPTIONS
607-6694	SUB ASSY,CPU SOCKET,K74,MOLEX	MOLEX_SOCKET
607-6693	SUB ASSY,CPU SOCKET,K74,FOXCONN	FOXCONN_SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
607-6694	1	MOLEX CPU SOCKET AND ILM	SKT_ILM	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
607-6693	607-6694		SKT_ILM	FOXCONN ALTERNATE

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3828	1	IC, IBEX PEAK PRQ, DESKTOP, FCBGA, PCH, P425	U1800	CRITICAL	
359S0157	1	IC, SL62AP108, CLK GEN, CK505, QFN3	U2600	CRITICAL	BUF_CLK
341T0230	1	IC, EFI BOOTROM, K74/K75	U6100	CRITICAL	
338S0765	1	IC, XI022112AY, 1394B_PCIE, PHY/LINK	U4100	CRITICAL	
825-7122	1	MLB LABEL, 48.0X4.8	X14	CRITICAL	
343S0493	1	IC, BCM5764M, ENET, 8X8	U3900	CRITICAL	BCM5764M
343S0494	1	IC, BCM57765A, ENET&SD, 8X8	U3900	CRITICAL	BCM57765
341T0269	1	ENET 1MBIT FLASH, CII, K74/K75	U3990	CRITICAL	BCM5764M
341T0246	1	ENET 1MBIT FLASH, CIV, K74/K75	U3990	CRITICAL	BCM57765

RAW: 335S0663

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3837	1	CKD,Q36R,Q5,2.93,73W,1333,C2,4M,LGA	CPU	CRITICAL	2P93GHZ_CKD_CPU
337S3912	1	CKD,SLBTD,PRQ,3.06,73W,1333,K0,4M,LGA	CPU	CRITICAL	3P86GHZ_CKD_CPU
337S3911	1	CKD,SLBUD,PRQ,3.20,73W,1333,K0,4M,LGA	CPU	CRITICAL	3P28GHZ_CKD_CPU
337S3900	1	CKD,SLBLT,PRQ,3.46,73W,1333,C2,4M,LGA	CPU	CRITICAL	3P46GHZ_CKD_CPU
337S3910	1	CKD,SLBTM,PRQ,3.60,73W,1333,K0,4M,LGA	CPU	CRITICAL	3P60GHZ_CKD_CPU
337S3862	1	LFD,Q36C,Q5,2.53,82W,1333,B1,8M,LGA	CPU	CRITICAL	2P53GHZ_LFD_CPU

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S3898	337S3912	3P06GHZ_CKD_CPU		C2, PRQ, 3.06 GHZ CKD

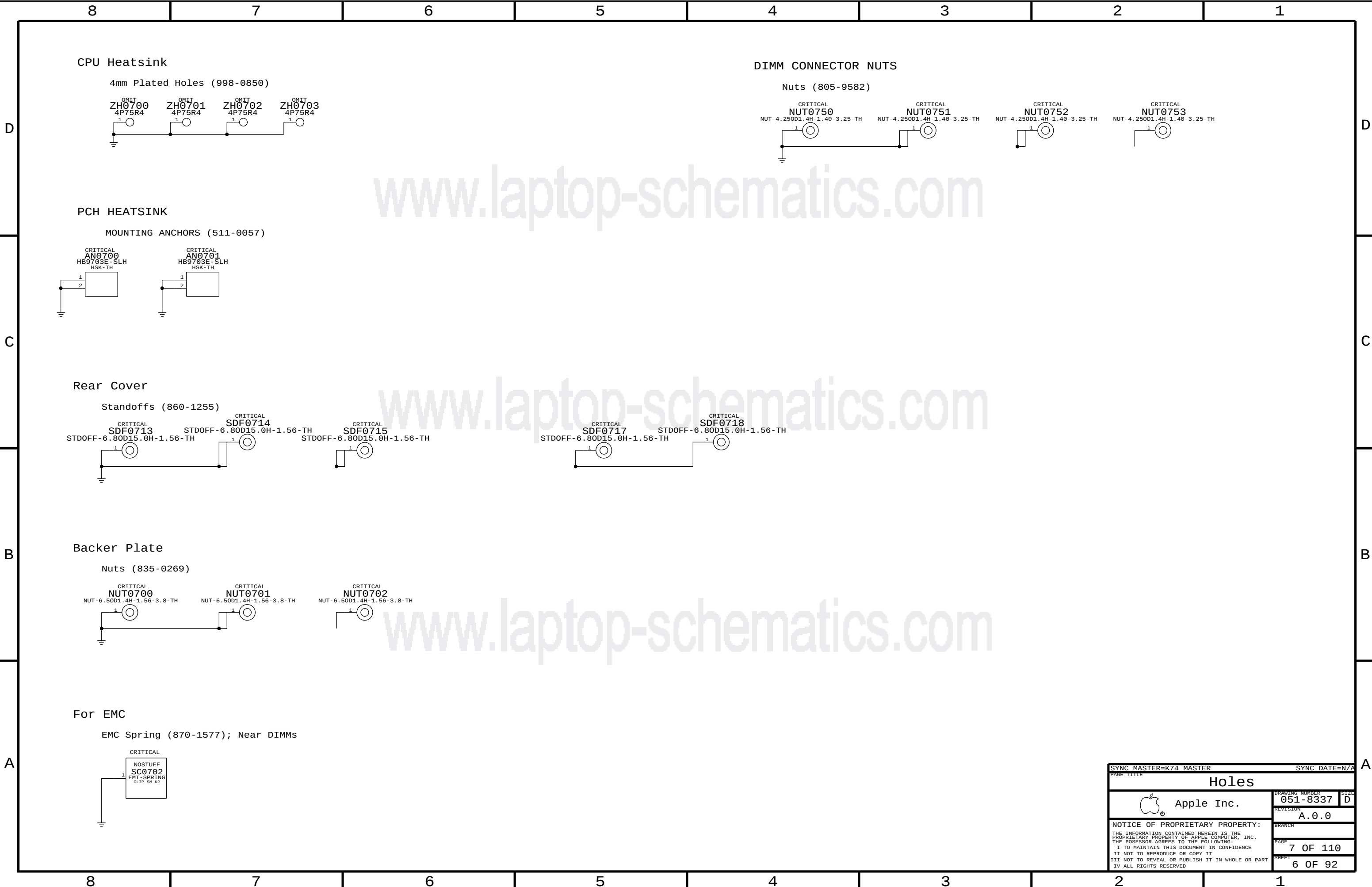
K74 PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8337	1	SCH, MLB, K74	SCH1		
820-2784	1	PCBF, MLB, K74	MLB1		
341T0231	1	IC, SMC, K74	U4900	CRITICAL	K74

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0339	197S0179		Y4190	FIREWIRE OSCILLATOR
128S0298	128S0293		C1670, C7260, C7444	

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BOM Configuration			
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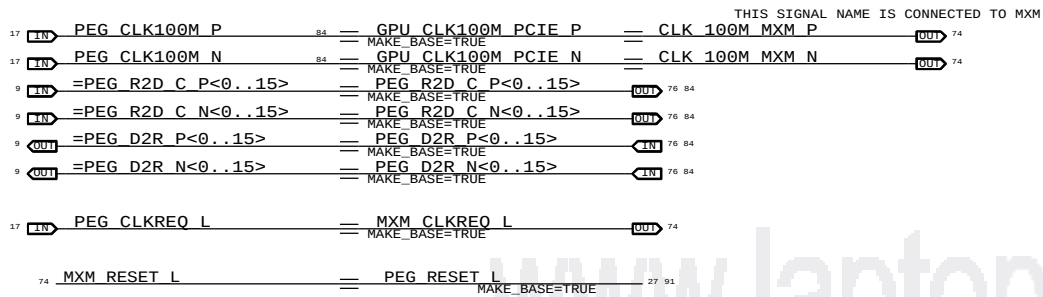
SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
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8	7	6	5	4	3	2	1
UNUSED CPU SIGNALS		NC ON UNUSED PCIE ALIASES		NC ON UNUSED DISPLAY ALIASES		NC ON UNUSED FDI ALIASES	
9 TP CPU RSVD<41..29> == NC CPU RSVD<41..29> MAKE_BASE=TRUE NO_TEST=TRUE		17 TP PCIE T28 D2R N<3..0> == NC PCIE T28 D2RN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE		18 TP CRT IG DDC CLK == NC CRT IG DDC CLK MAKE_BASE=TRUE NO_TEST=TRUE		9 TP CPU FDI TX N<7..0> == NC CPU FDI TXN<7..0> MAKE_BASE=TRUE NO_TEST=TRUE	
9 TP CPU RSVD<26..1> == NC CPU RSVD<26..1> MAKE_BASE=TRUE NO_TEST=TRUE		17 TP PCIE T28 D2R P<3..0> == NC PCIE T28 D2RP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE		18 TP CRT IG DDC DATA == NC CRT IG DDC DATA MAKE_BASE=TRUE NO_TEST=TRUE		9 TP CPU FDI TX P<7..0> == NC CPU FDI TXP<7..0> MAKE_BASE=TRUE NO_TEST=TRUE	
12 TP CPU FC AE38 == NC CPU FC AE38 MAKE_BASE=TRUE NO_TEST=TRUE		17 TP PCIE T28 R2D C N<3..0> == NC PCIE T28 R2D CN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE		18 TP CRT IG RED == NC CRT IG RED MAKE_BASE=TRUE NO_TEST=TRUE		18 TP PCH FDI RX N<7..0> == NC PCH FDI RXN<7..0> MAKE_BASE=TRUE NO_TEST=TRUE	
12 TP CPU FC AG40 == NC CPU FC AG40 MAKE_BASE=TRUE NO_TEST=TRUE		17 TP PCIE T28 R2D C P<3..0> == NC PCIE T28 R2D CP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE		18 TP CRT IG GREEN == NC CRT IG GREEN MAKE_BASE=TRUE NO_TEST=TRUE		18 TP PCH FDI RX P<7..0> == NC PCH FDI RXP<7..0> MAKE_BASE=TRUE NO_TEST=TRUE	
NC ON UNUSED PCI ALIASES		17 TP PCIE CLK100M T28 N == NC PCIE CLK100M T28N MAKE_BASE=TRUE NO_TEST=TRUE		18 TP CRT IG BLUE == NC CRT IG BLUE MAKE_BASE=TRUE NO_TEST=TRUE		9 TP CPU FDI FSYNC<1..0> == NC CPU FDI FSYNC<1..0> MAKE_BASE=TRUE NO_TEST=TRUE	
19 TP PCI AD<31..0> == NC PCI AD<31..0> MAKE_BASE=TRUE NO_TEST=TRUE		17 TP PCIE CLK100M T28 P == NC PCIE CLK100M T28P MAKE_BASE=TRUE NO_TEST=TRUE		18 TP CRT IG HSYNC == NC CRT IG HSYNC MAKE_BASE=TRUE NO_TEST=TRUE		18 TP PCH FDI FSYNC<1..0> == NC PCH FDI FSYNC<1..0> MAKE_BASE=TRUE NO_TEST=TRUE	
19 TP PCI C BE L<3..0> == NC PCI C BE L<3..0> MAKE_BASE=TRUE NO_TEST=TRUE		17 PCIE EXCARD D2R P == NC PCIE EXCARD D2RP MAKE_BASE=TRUE NO_TEST=TRUE		18 TP CRT IG VSYNC == NC CRT IG VSYNC MAKE_BASE=TRUE NO_TEST=TRUE		9 TP CPU FDI LSYNC<1..0> == NC CPU FDI LSYNC<1..0> MAKE_BASE=TRUE NO_TEST=TRUE	
19 TP PCI PAR == NC PCI PAR MAKE_BASE=TRUE NO_TEST=TRUE		17 PCIE EXCARD D2R N == NC PCIE EXCARD D2RN MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG B MLN<3..0> == NC DP IG B MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE		18 TP PCH FDI LSYNC<1..0> == NC PCH FDI LSYNC<1..0> MAKE_BASE=TRUE NO_TEST=TRUE	
19 TP PCI RESET L == NC PCI RESET L MAKE_BASE=TRUE NO_TEST=TRUE		17 PCIE EXCARD R2D C P == NC PCIE EXCARD R2D CP MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG B MLP<3..0> == NC DP IG B MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE		9 TP CPU FDI INT == NC CPU FDI INT MAKE_BASE=TRUE NO_TEST=TRUE	
20 TP PCIE CLK100M XDPP == NC PCIE CLK100M XDPP MAKE_BASE=TRUE NO_TEST=TRUE		17 PCIE EXCARD R2D C N == NC PCIE EXCARD R2D CN MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG B AUX N == NC DP IG B AUXN MAKE_BASE=TRUE NO_TEST=TRUE		18 TP PCH FDI INT == NC PCH FDI INT MAKE_BASE=TRUE NO_TEST=TRUE	
20 TP PCIE CLK100M XDPN == NC PCIE CLK100M XDPN MAKE_BASE=TRUE NO_TEST=TRUE		17 PCIE CLK100M EXCARD P == NC PCIE CLK100M EXCARDP MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG B AUX P == NC DP IG B AUXP MAKE_BASE=TRUE NO_TEST=TRUE			
20 TP DMI CLK100M LAP == NC DMI CLK100M LAP MAKE_BASE=TRUE NO_TEST=TRUE		17 PCIE CLK100M EXCARD N == NC PCIE CLK100M EXCARDN MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG B HPD == NC DP IG B HPD MAKE_BASE=TRUE NO_TEST=TRUE			
20 TP DMI CLK100M LAN == NC DMI CLK100M LAN MAKE_BASE=TRUE NO_TEST=TRUE		17 TP PCIE CLK100M PE5P == NC PCIE CLK100M PE5P MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG B DDC_CLK == NC DP IG B DDC_CLK MAKE_BASE=TRUE NO_TEST=TRUE			
17 TP LPC DRE01 L == NC LPC DRE01 L MAKE_BASE=TRUE NO_TEST=TRUE		17 TP PCIE CLK100M PE5N == NC PCIE CLK100M PE5N MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG B DDC DATA == NC DP IG B DDC_DATA MAKE_BASE=TRUE NO_TEST=TRUE			
17 TP LPC DRE00 L == NC LPC DRE00 L MAKE_BASE=TRUE NO_TEST=TRUE		17 DMI MIDBUS CLK100M P == NC DMI MIDBUS CLK100MP MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG C MLN<3..0> == NC DP IG C MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE			
17 TP LPC DRE00 L == NC LPC DRE00 L MAKE_BASE=TRUE NO_TEST=TRUE		17 DMI MIDBUS CLK100M N == NC DMI MIDBUS CLK100MN MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG C MLP<3..0> == NC DP IG C MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE			
NC ON UNUSED NAND ALIASES		NC ON UNUSED USB ALIASES		18 TP DP IG C AUX N == NC DP IG C AUXN MAKE_BASE=TRUE NO_TEST=TRUE		NC ON UNUSED SATA ALIASES	
19 TP NV CE L<3..0> == NC NV CE L<3..0> MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 1N == NC USB 1N MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG C AUX P == NC DP IG C AUXP MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA D D2RN == NC SATA D D2RN MAKE_BASE=TRUE NO_TEST=TRUE	
19 TP NV DQS<1..0> == NC NV DQS<1..0> MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 1P == NC USB 1P MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG C HPD == NC DP IG C HPD MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA D D2RP == NC SATA D D2RP MAKE_BASE=TRUE NO_TEST=TRUE	
19 TP NV DQ<15..0> == NC NV DQ<15..0> MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 2N == NC USB 2N MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG C CTRL_CLK == NC DP IG C CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA D R2D CN == NC SATA D R2D CN MAKE_BASE=TRUE NO_TEST=TRUE	
19 TP NV RCOMP == NC NV RCOMP MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 2P == NC USB 2P MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG C CTRL_DATA == NC DP IG C CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA D R2D CP == NC SATA D R2D CP MAKE_BASE=TRUE NO_TEST=TRUE	
19 TP NV RB L == NC NV RB L MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 3N == NC USB 3N MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG D MLN<3..0> == NC DP IG D MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA E D2RN == NC SATA E D2RN MAKE_BASE=TRUE NO_TEST=TRUE	
19 TP NV WR RE L<1..0> == NC NV WR RE L<1..0> MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 3P == NC USB 3P MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG D MLP<3..0> == NC DP IG D MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA E D2RP == NC SATA E D2RP MAKE_BASE=TRUE NO_TEST=TRUE	
19 TP NV WE CK L<1..0> == NC NV WE CK L<1..0> MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 4N == NC USB 4N MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG D AUXN == NC DP IG D AUXN MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA E R2D CN == NC SATA E R2D CN MAKE_BASE=TRUE NO_TEST=TRUE	
19 TP NV ALE == NC NV ALE MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 4P == NC USB 4P MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG D AUXP == NC DP IG D AUXP MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA E R2D CP == NC SATA E R2D CP MAKE_BASE=TRUE NO_TEST=TRUE	
19 TP NV CLE == NC NV CLE MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 5N == NC USB 5N MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG D HPD == NC DP IG D HPD MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA F D2RN == NC SATA F D2RN MAKE_BASE=TRUE NO_TEST=TRUE	
NC ON UNUSED MEM ALIASES		19 TP USB 5P == NC USB 5P MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG D CTRL_CLK == NC DP IG D CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA F D2RP == NC SATA F D2RP MAKE_BASE=TRUE NO_TEST=TRUE	
11 TP MEM A CS L<7..4> == NC MEM A CS L<7..4> MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 6N == NC USB 6N MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG D CTRL_DATA == NC DP IG D CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA F R2D CN == NC SATA F R2D CN MAKE_BASE=TRUE NO_TEST=TRUE	
11 TP MEM A DQ CB<7..0> == NC MEM A DQ CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 6P == NC USB 6P MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG D CTRL_CLK == NC DP IG D CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA F R2D CP == NC SATA F R2D CP MAKE_BASE=TRUE NO_TEST=TRUE	
11 TP MEM A DQS N<8> == NC MEM A DQSN<8> MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 7N == NC USB 7N MAKE_BASE=TRUE NO_TEST=TRUE		18 TP DP IG D CTRL_DATA == NC DP IG D CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA SSD D2RN == NC SATA SSD D2RN MAKE_BASE=TRUE NO_TEST=TRUE	
11 TP MEM A DQS P<8> == NC MEM A DQSP<8> MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 7P == NC USB 7P MAKE_BASE=TRUE NO_TEST=TRUE		18 TP SDVO TVCLKINN == NC SDVO TVCLKINN MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA SSD D2R P == NC SATA SSD D2RP MAKE_BASE=TRUE NO_TEST=TRUE	
11 TP MEM B CS L<7..4> == NC MEM B CS L<7..4> MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 9N == NC USB 9N MAKE_BASE=TRUE NO_TEST=TRUE		18 TP SDVO STALLN == NC SDVO STALLN MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA SSD R2D C N == NC SATA SSD R2D CN MAKE_BASE=TRUE NO_TEST=TRUE	
11 TP MEM B DQ CB<7..0> == NC MEM B DQ CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 9P == NC USB 9P MAKE_BASE=TRUE NO_TEST=TRUE		18 TP SDVO STALLP == NC SDVO STALLP MAKE_BASE=TRUE NO_TEST=TRUE		17 TP SATA SSD R2D C P == NC SATA SSD R2D CP MAKE_BASE=TRUE NO_TEST=TRUE	
11 TP MEM B DQS N<8> == NC MEM B DQSN<8> MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 10N == NC USB 10N MAKE_BASE=TRUE NO_TEST=TRUE		18 TP SDVO INTN == NC SDVO INTN MAKE_BASE=TRUE NO_TEST=TRUE			
11 TP MEM B DQS P<8> == NC MEM B DQSP<8> MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 10P == NC USB 10P MAKE_BASE=TRUE NO_TEST=TRUE		18 TP SDVO INTP == NC SDVO INTP MAKE_BASE=TRUE NO_TEST=TRUE			
NC ON UNUSED MISC ALIASES		19 TP USB 11N == NC USB 11N MAKE_BASE=TRUE NO_TEST=TRUE					
17 TP HDA SDIN1 == NC HDA SDIN1 MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 11P == NC USB 11P MAKE_BASE=TRUE NO_TEST=TRUE					
17 TP HDA SDIN2 == NC HDA SDIN2 MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 12N == NC USB 12N MAKE_BASE=TRUE NO_TEST=TRUE					
17 TP HDA SDIN3 == NC HDA SDIN3 MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 12P == NC USB 12P MAKE_BASE=TRUE NO_TEST=TRUE					
TP JTAG XDP TRST L == NC JTAG XDP TRST L MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 13N == NC USB 13N MAKE_BASE=TRUE NO_TEST=TRUE					
20 TP PCH PWM0 == NC PCH PWM0 MAKE_BASE=TRUE NO_TEST=TRUE		19 TP USB 13P == NC USB 13P MAKE_BASE=TRUE NO_TEST=TRUE					
20 TP PCH PWM1 == NC PCH PWM1 MAKE_BASE=TRUE NO_TEST=TRUE							
20 TP PCH PWM2 == NC PCH PWM2 MAKE_BASE=TRUE NO_TEST=TRUE							
20 TP PCH PWM3 == NC PCH PWM3 MAKE_BASE=TRUE NO_TEST=TRUE							
20 TP PCH SST == NC PCH SST MAKE_BASE=TRUE NO_TEST=TRUE							
9 SNS CPU THERMD N == NC SNS CPU THERMDN MAKE_BASE=TRUE NO_TEST=TRUE							
9 SNS CPU THERMD P == NC SNS CPU THERMDP MAKE_BASE=TRUE NO_TEST=TRUE							
8	7	6	5	4	3	2	1

SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE		UNUS	
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		REVISION	A.0.0
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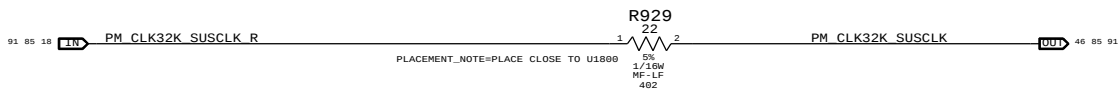
www.laptop-schematics.com

PEG Slot Support

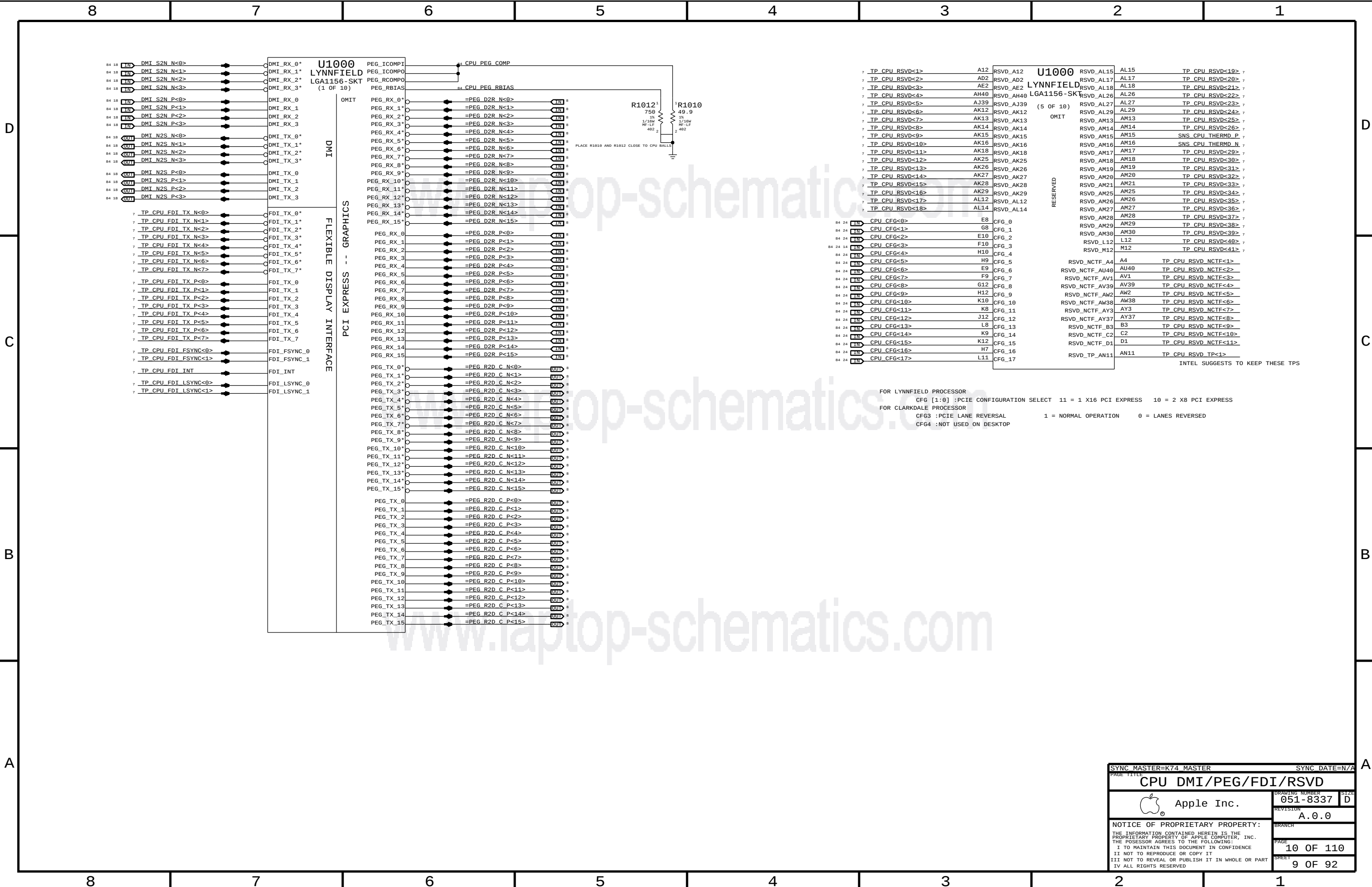


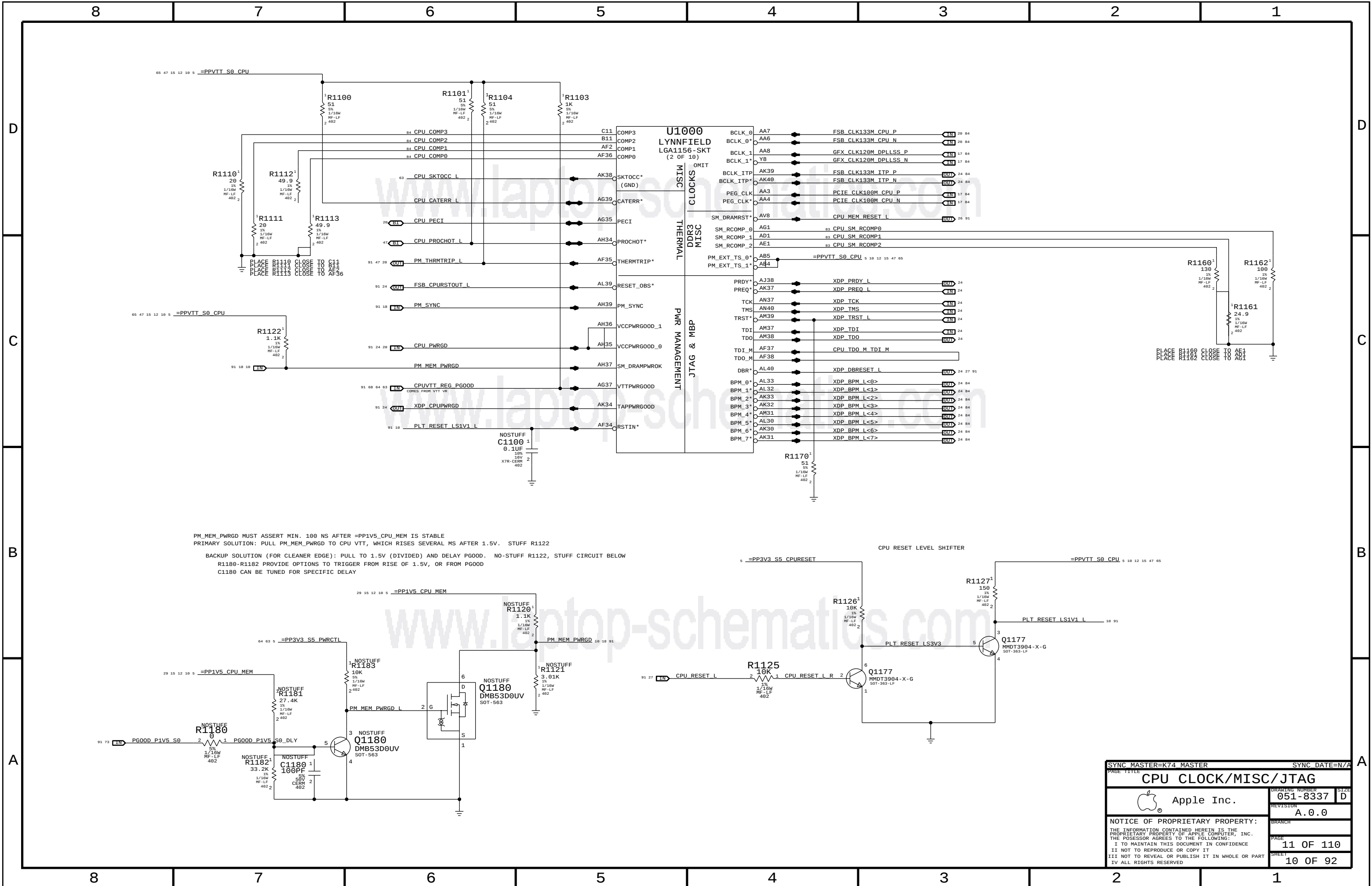
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www.laptop-schematics.com



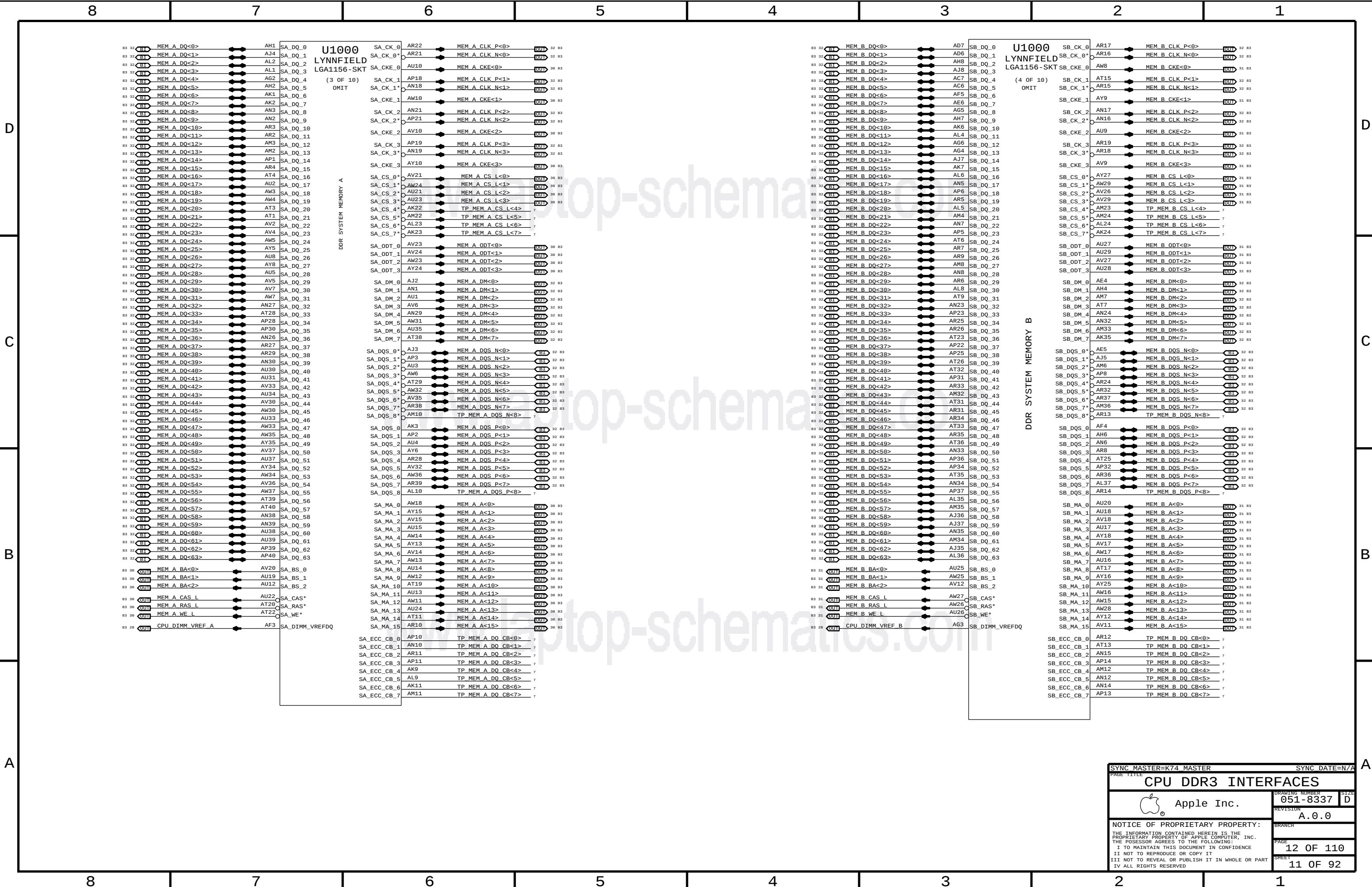
SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE		Signal Aliases	
Apple Inc.		DRAWING NUMBER	051-8337
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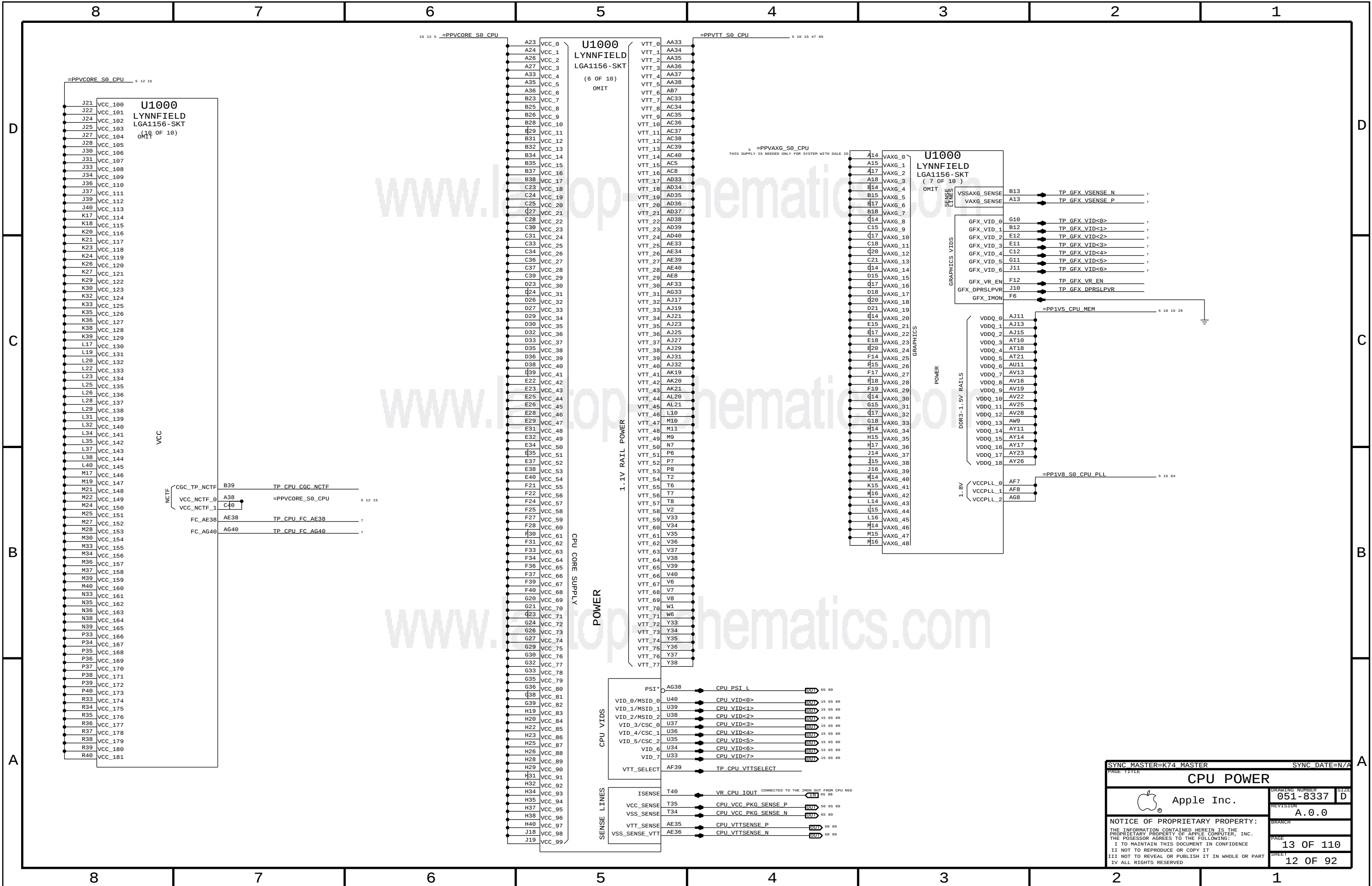




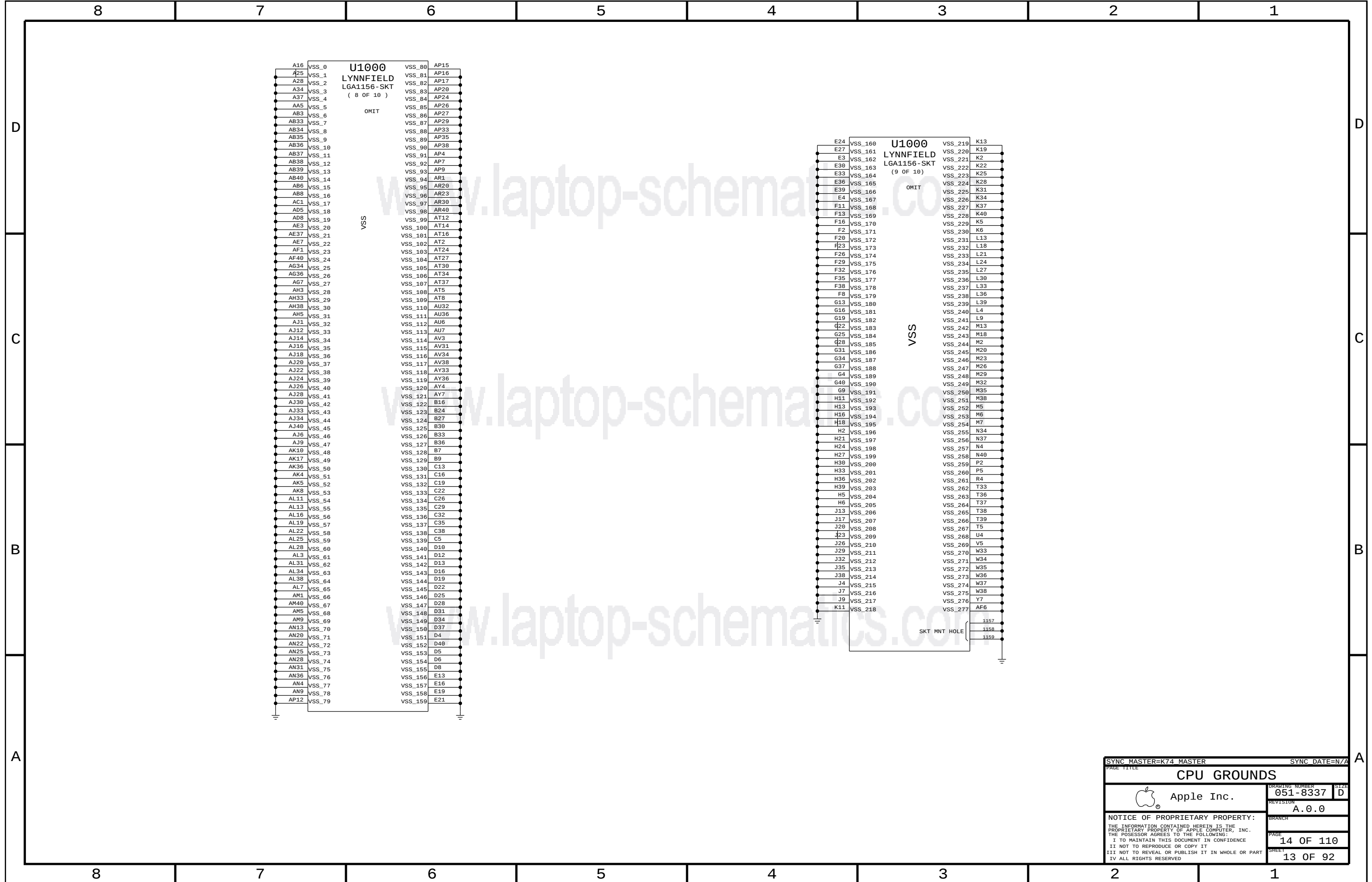
PM_MEM_PWRGD MUST ASSERT MIN. 100 NS AFTER =PP1V5_CPU_MEM IS STABLE
PRIMARY SOLUTION: PULL PM_MEM_PWRGD TO CPU VTT, WHICH RISES SEVERAL MS AFTER 1.5V. STUFF R1122
BACKUP SOLUTION (FOR CLEANER EDGE): PULL TO 1.5V (DIVIDED) AND DELAY PG00D. NO-STUFF R1122, STUFF CIRCUIT BELOW
R1180-R1182 PROVIDE OPTIONS TO TRIGGER FROM RISE OF 1.5V, OR FROM PG00D
C1180 CAN BE TUNED FOR SPECIFIC DELAY

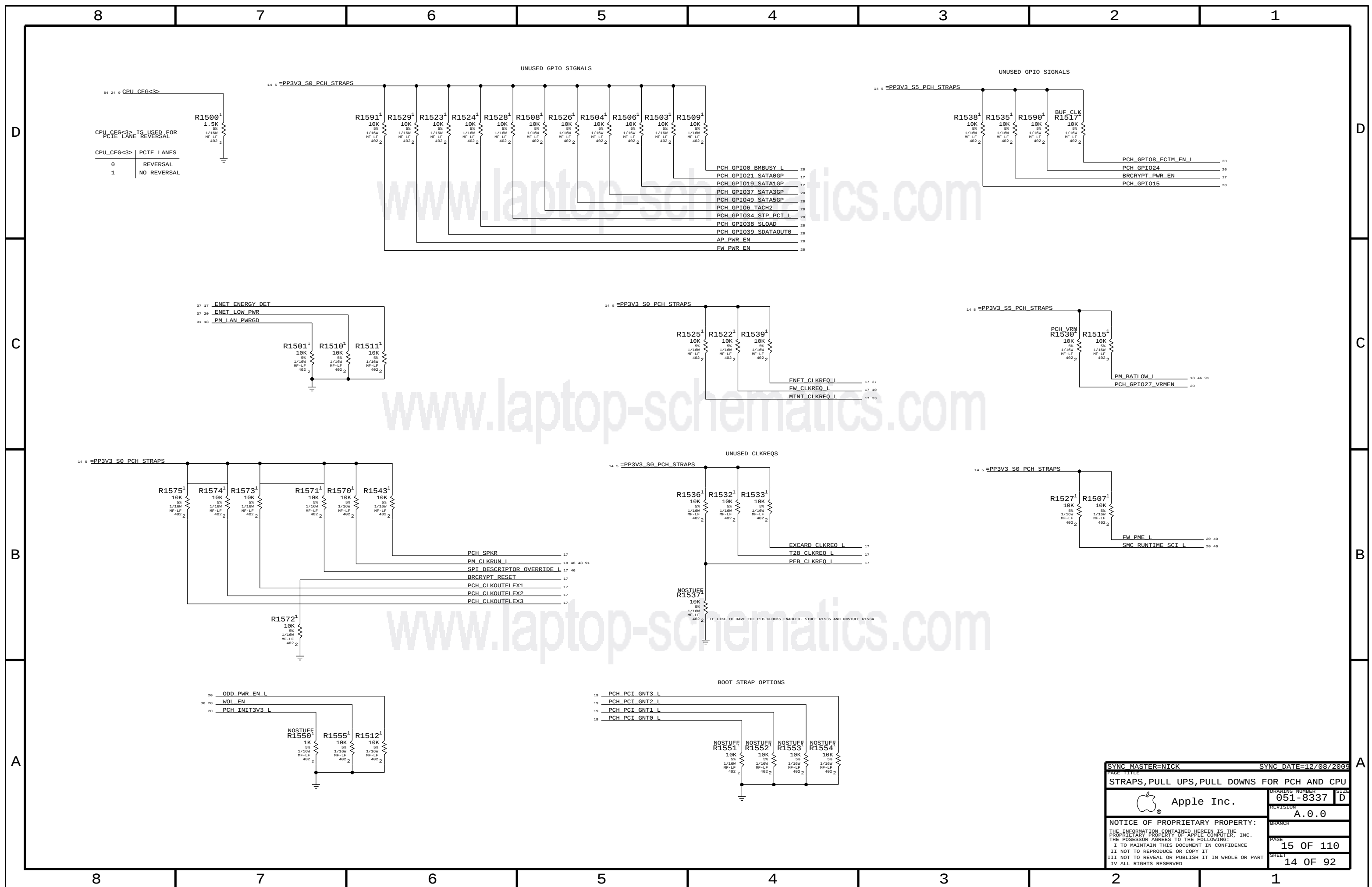
PAGE TITLE		SYNC DATE=N/A	
CPU CLOCK/MISC/JTAG		DRAWING NUMBER	
Apple Inc.		051-8337	
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		10 OF 92	





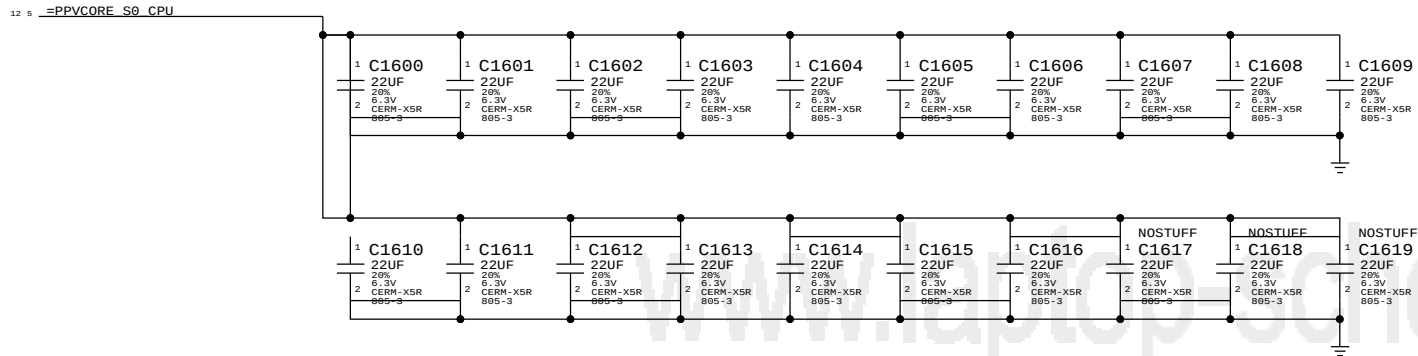
SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE		CPU POWER	
 Apple Inc.		DRAWING NUMBER	051-8337
		REVISION	A.0.0
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		PAGE	13 OF 110
		SHEET	12 OF 92





CPU VCORE DECOUPLING

INTEL RECOMMENDATION 17X 22UF 0805



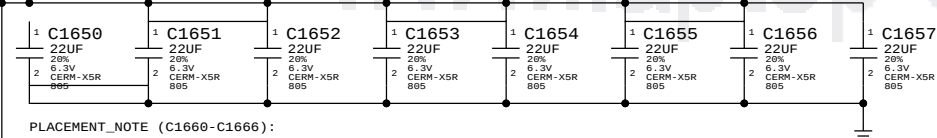
BULK CAPS ON CPU VREG PAGE 74

VTT (CPU Uncore) DECOUPLING

8X 22UF 0805, 7X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805

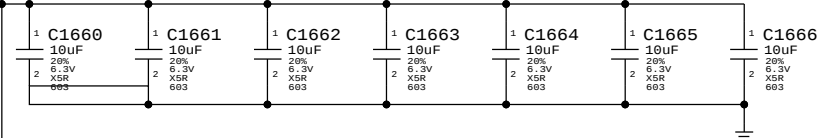
PLACEMENT_NOTE (C1650-C1657):

Place under socket cavity on secondary side.

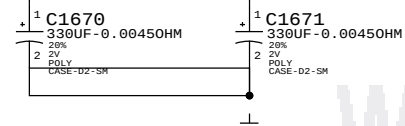


PLACEMENT_NOTE (C1660-C1666):

Place at edge of socket.

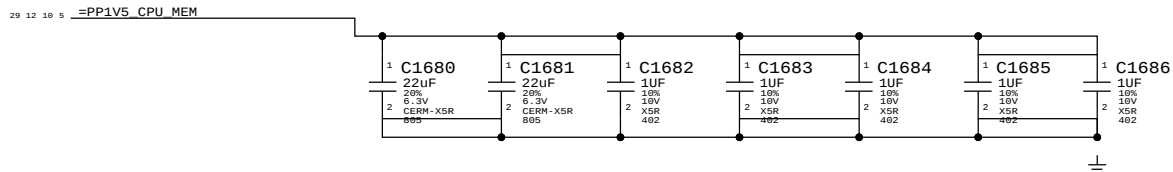


BULK CAPS ON CPU VTT REG PAGE 74



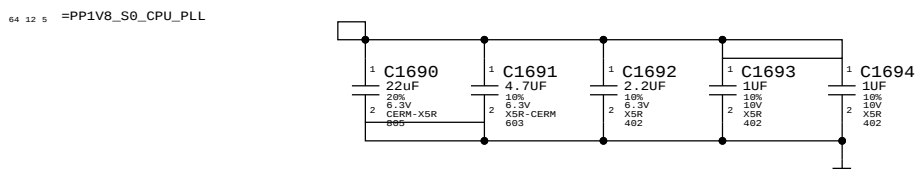
Memory (CPU VCCDDR) DECOUPLING

2x 22uF 0805, 5x 1uF 0402



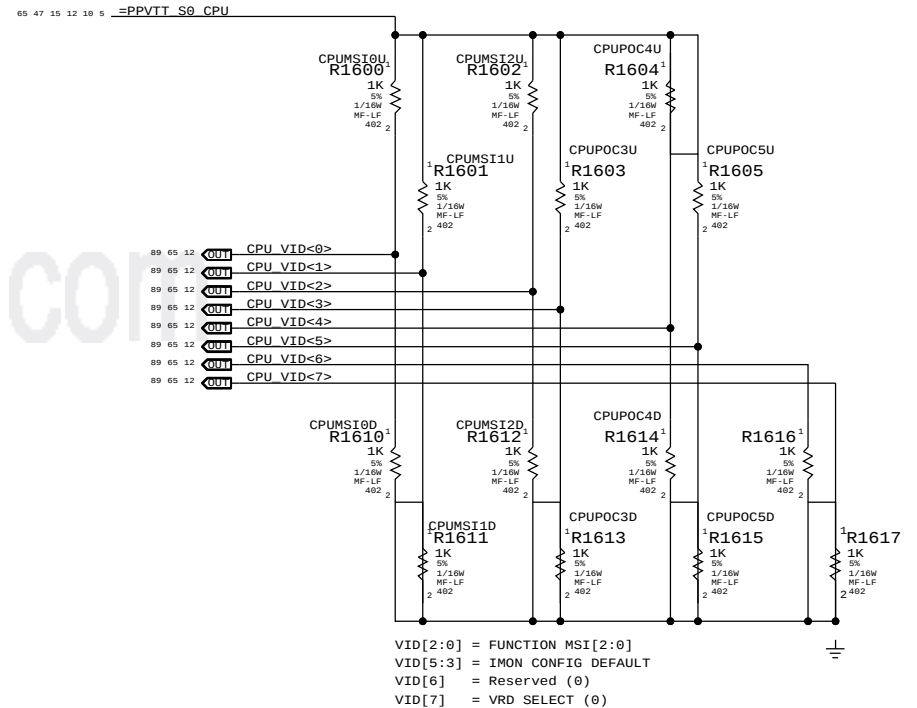
PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402



CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout



VID[2:0] = FUNCTION MSI[2:0]
VID[5:3] = IMON CONFIG DEFAULT
VID[6] = Reserved (0)
VID[7] = VRD SELECT (0)

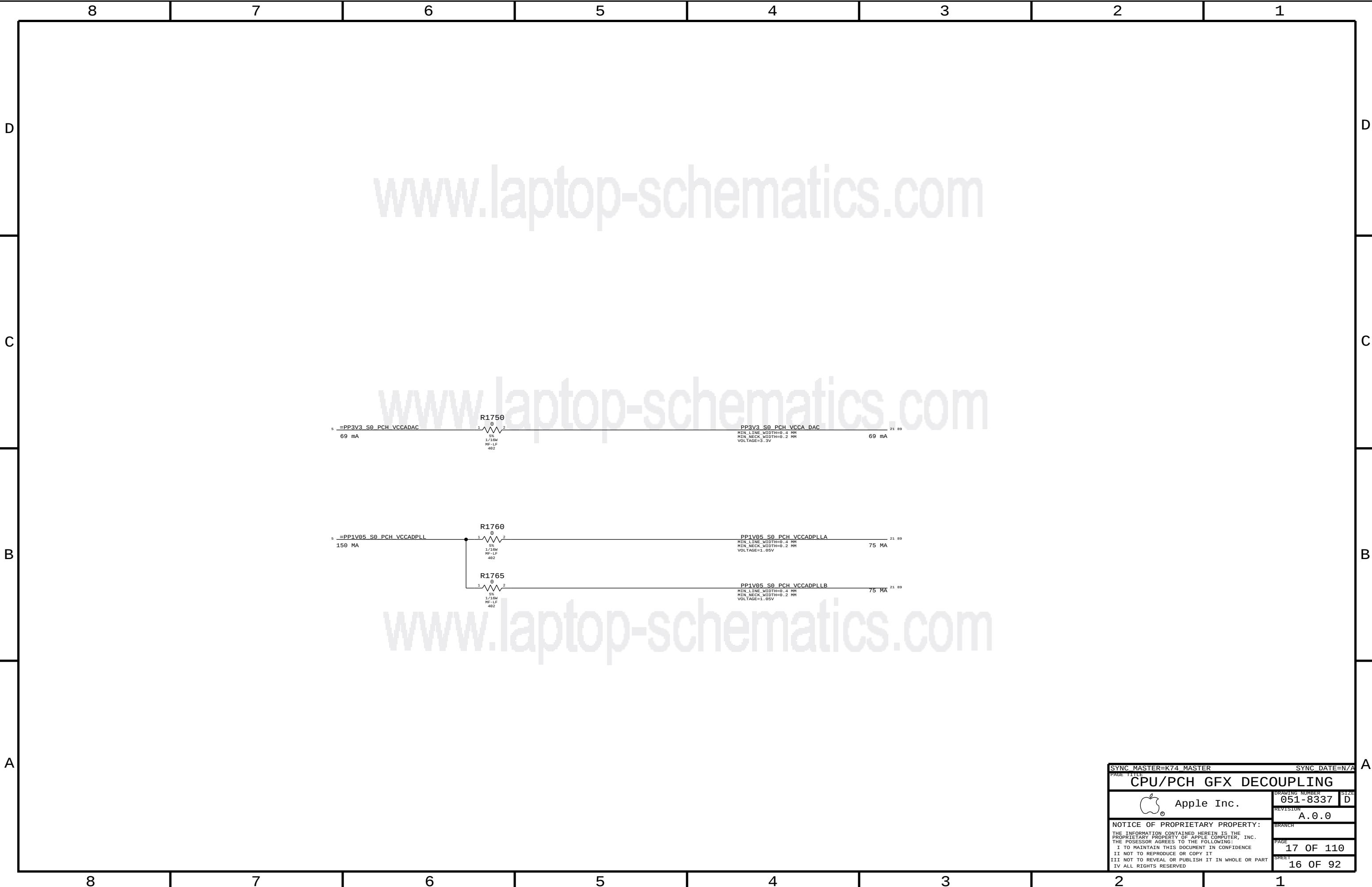
MSI - MARKET SEGMENT IDENTIFICATION
PREVENTS THE PLATFORM BOOTING USING A HIGHER POWERED CPU

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC5D, CPUPOC4D, CPUPOC3D	
CPUPOC_IMAX_0_40	40A	001	CPUPOC5D, CPUPOC4D, CPUPOC3U	45
CPUPOC_IMAX_40_60	60A	010	CPUPOC5D, CPUPOC4U, CPUPOC3D	30
CPUPOC_IMAX_60_80	80A	011	CPUPOC5D, CPUPOC4U, CPUPOC3U	22.5
CPUPOC_IMAX_80_100	100A	100	CPUPOC5U, CPUPOC4D, CPUPOC3D	18
CPUPOC_IMAX_100_120	120A	101	CPUPOC5U, CPUPOC4D, CPUPOC3U	15
CPUPOC_IMAX_120_140	140A	110	CPUPOC5U, CPUPOC4U, CPUPOC3D	12.857
CPUPOC_IMAX_140_180	180A	111	CPUPOC5U, CPUPOC4U, CPUPOC3U	10

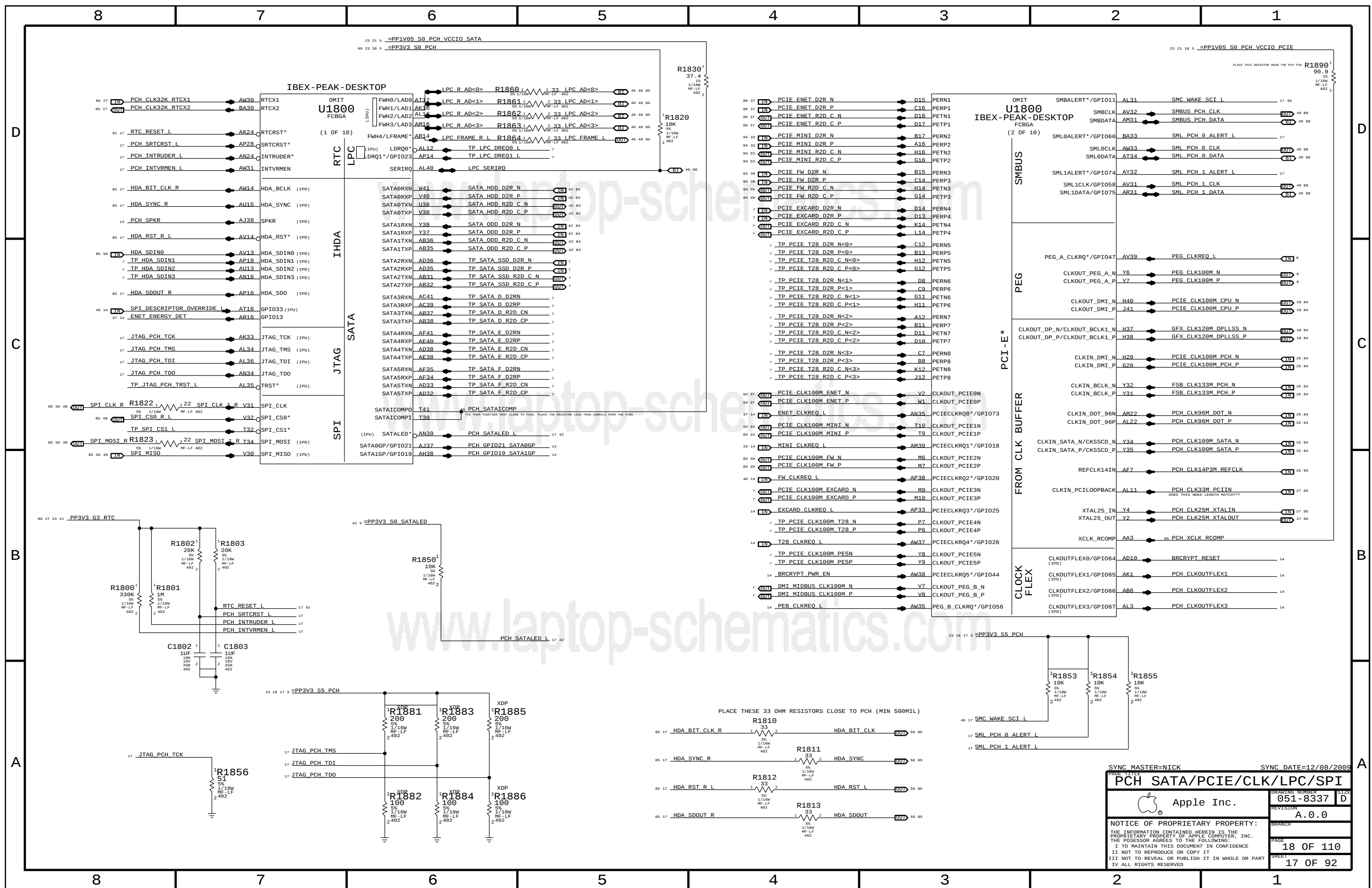
BOM GROUP	BOM OPTIONS
CLARKDALE_73W	CKD, CPUPOC_IMAX_60_80, CPUMSI2U, CPUMSI1D, CPUMSI0U
LYNNFIELD_82W	LFD, CPUPOC_IMAX_60_80, CPUMSI2U, CPUMSI1D, CPUMSI0U
LYNNFIELD_95W	LFD, CPUPOC_IMAX_100_120, CPUMSI2U, CPUMSI1U, CPUMSI0D

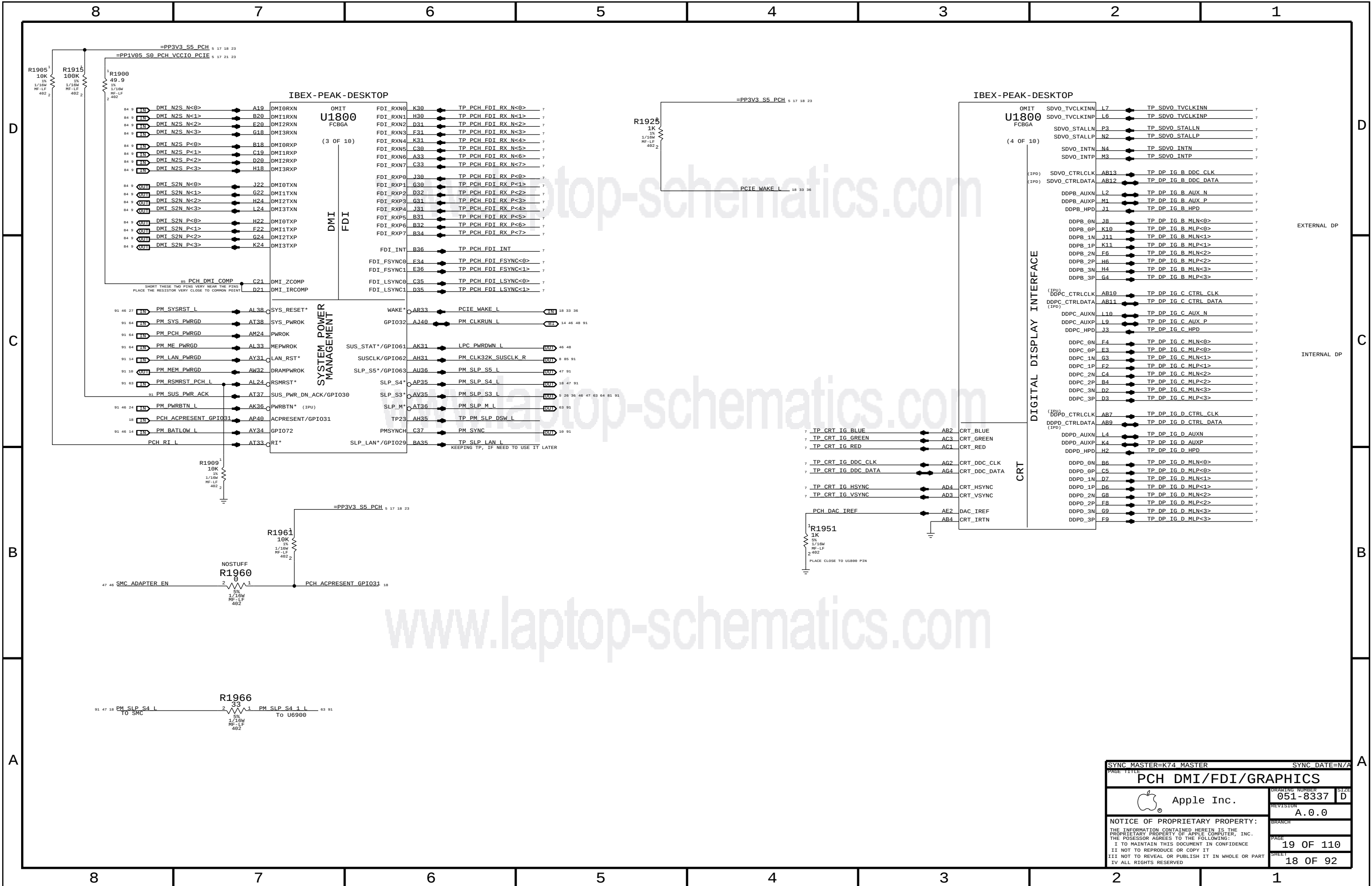
NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONS directly.
Instead call out appropriate BOM GROUP defined in tables above.

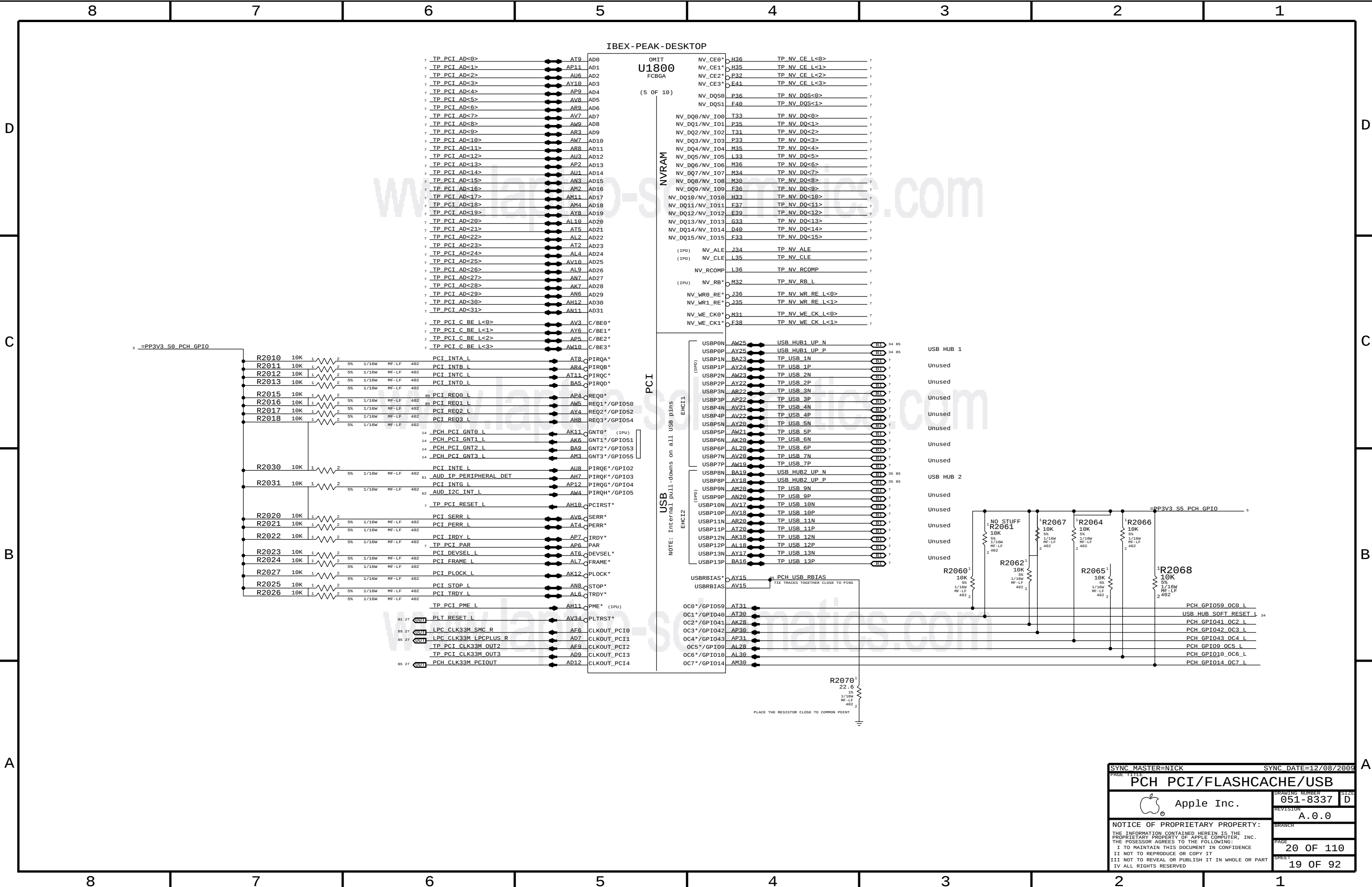
SYNC MASTER=NICK		SYNC DATE=12/08/2009	
PAGE TITLE			
CPU NON-GFX DECOUPLING			
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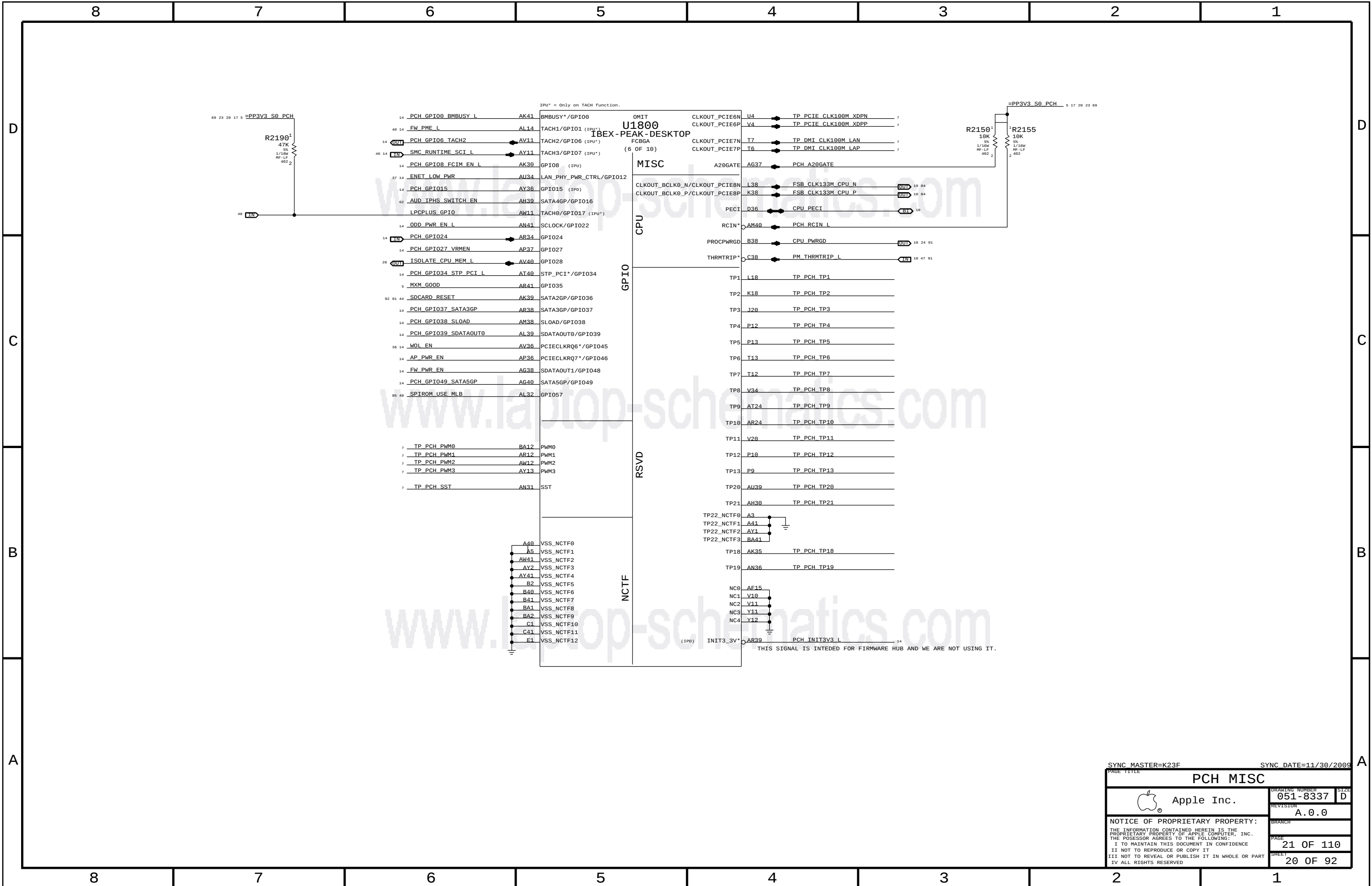


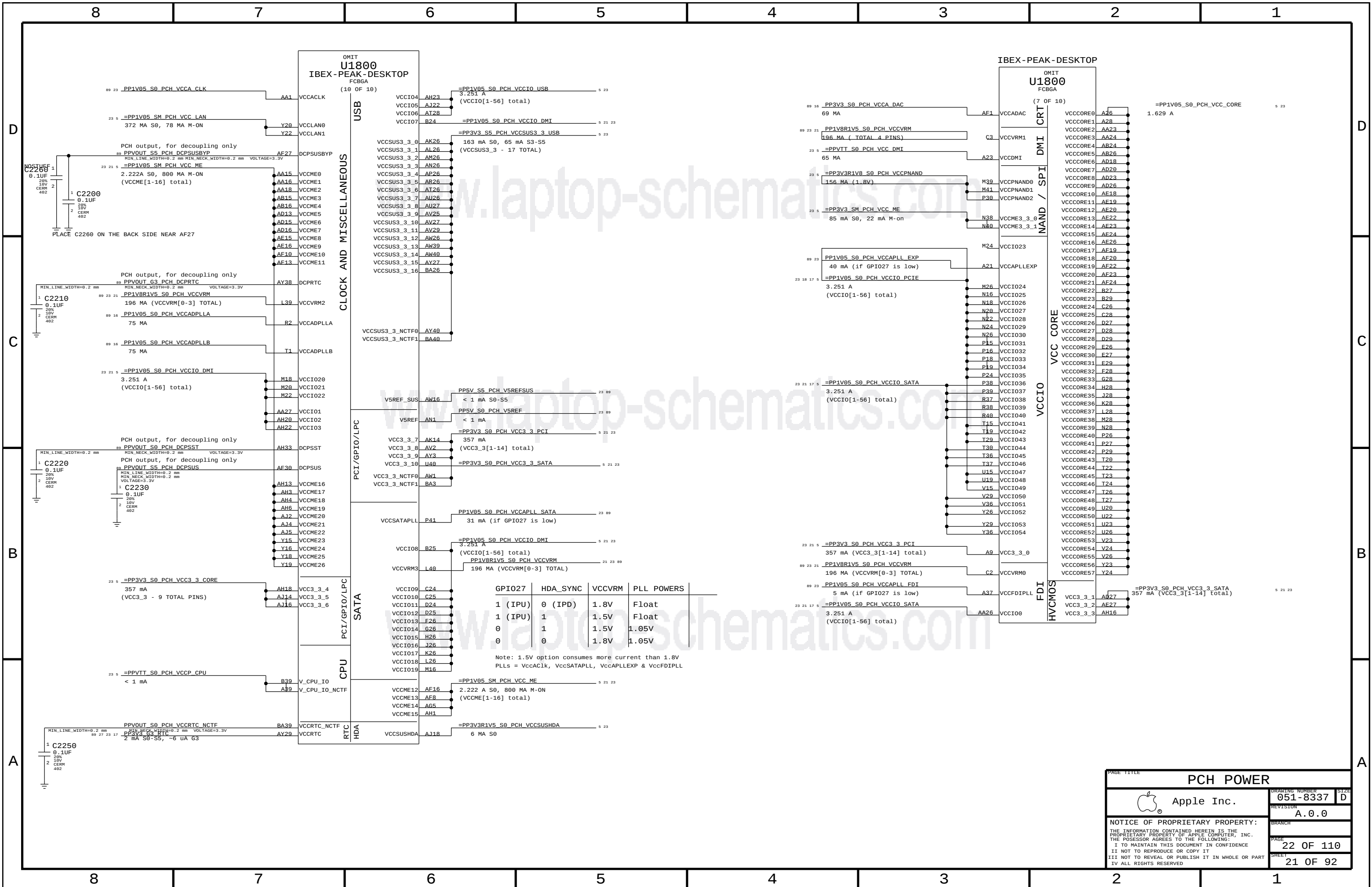
SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE			
CPU/PCH GFX DECOUPLING			
 Apple Inc.		DRAWING NUMBER	051-8337
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		SHEET	16 OF 92

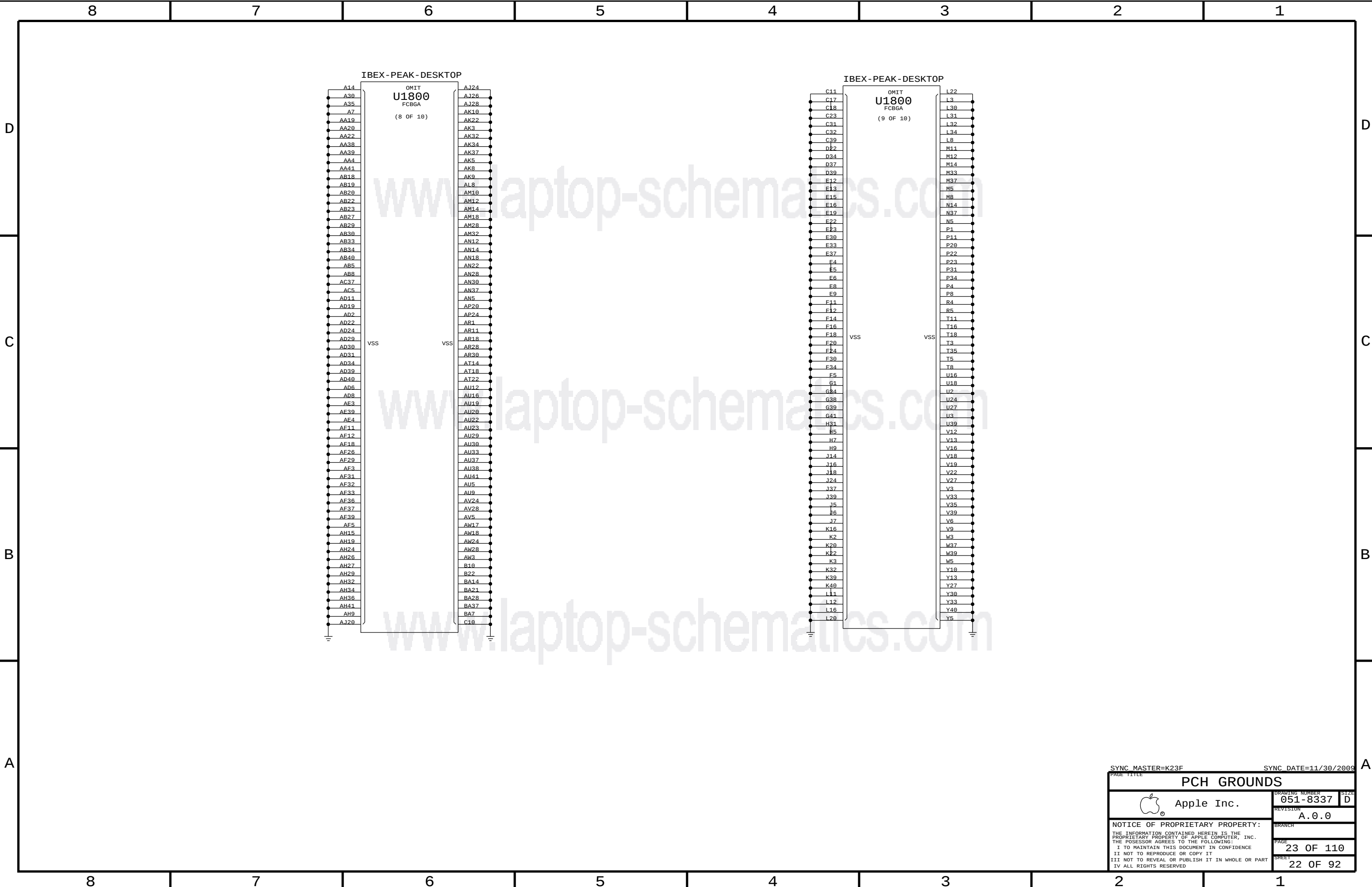




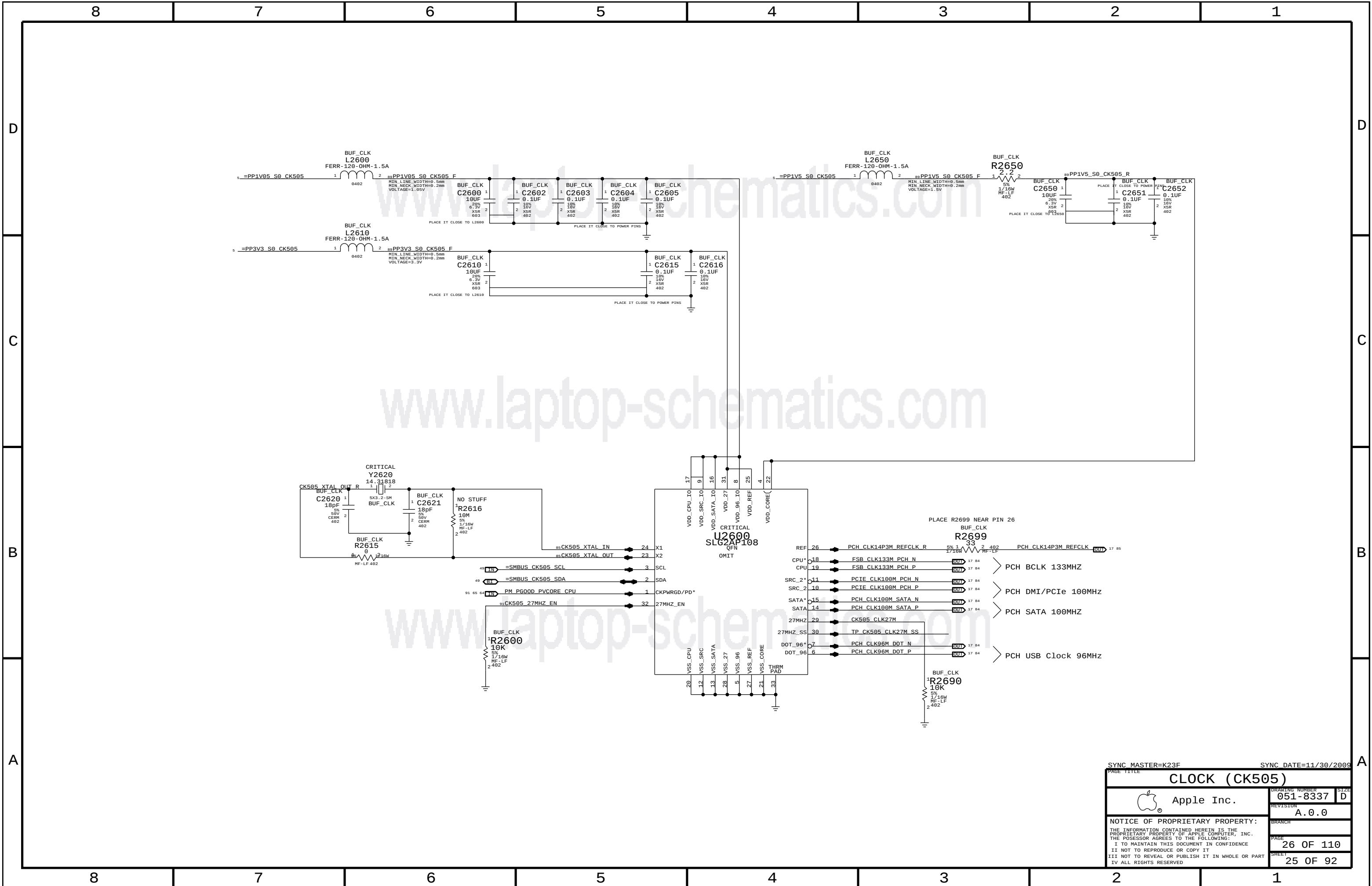












SYNC MASTER=K23F

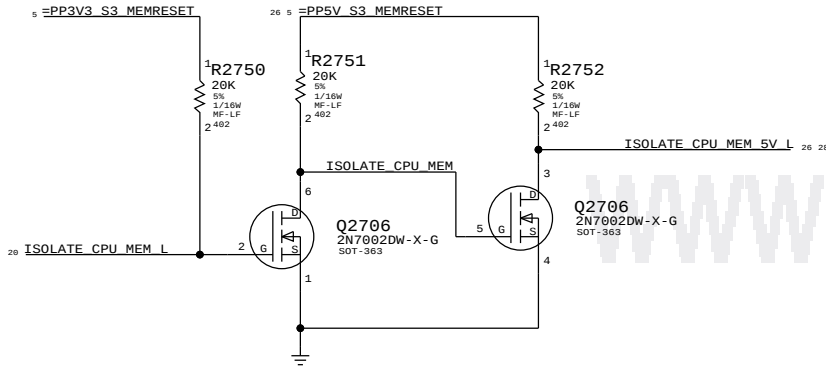
SYNC DATE=11/30/2009

PAGE TITLE		CLOCK (CK505)	
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		BRANCH	
		PAGE	26 OF 110
		SHEET	25 OF 92

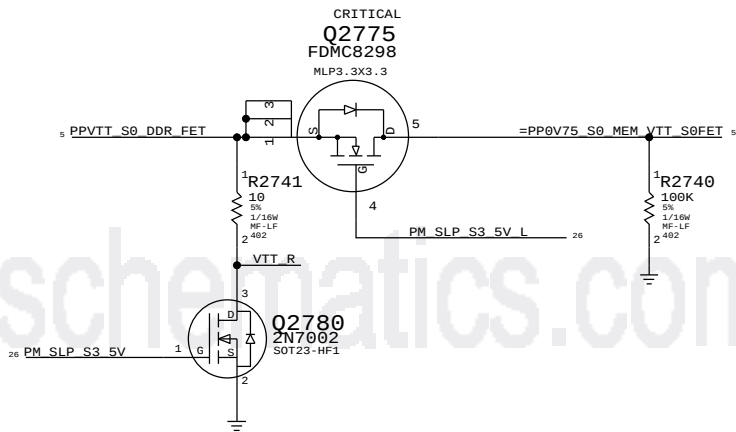
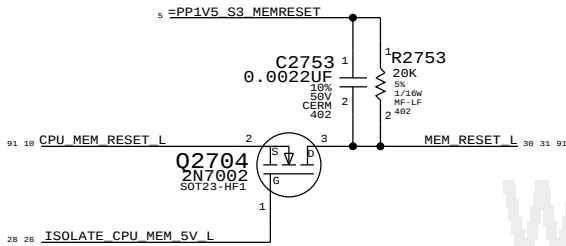
DDR3 RESET Support

LFD CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.

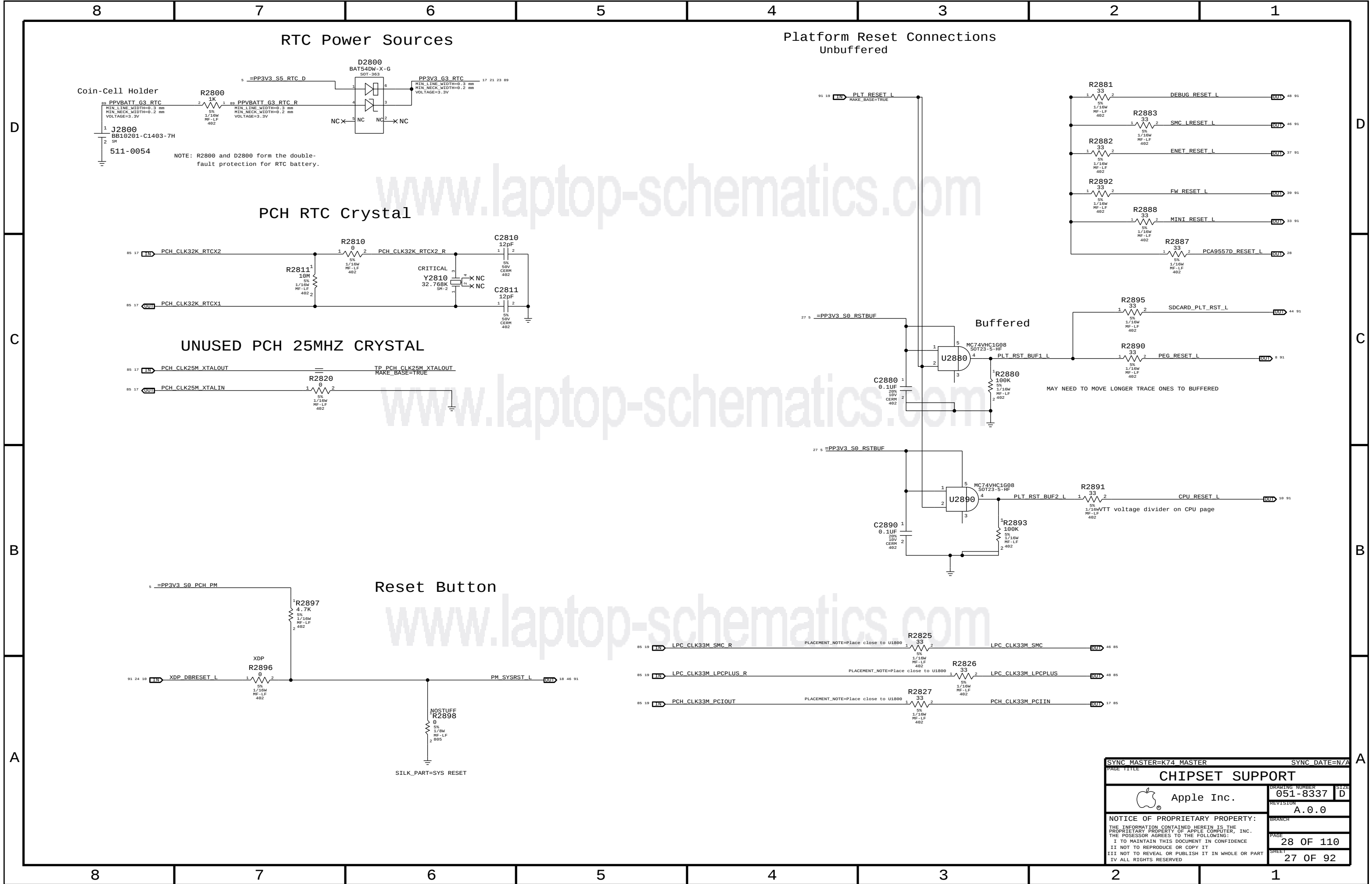
BUFFER ISOLATE_CPU_MEM_L TO 5V



MEM RESET ISOLATION



	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0



SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE			
CHIPSET SUPPORT			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-8337		D
REVISION			
A.0.0			
BRANCH			
PAGE			
28 OF 110			
SHEET			
27 OF 92			

Power aliases required by this page:

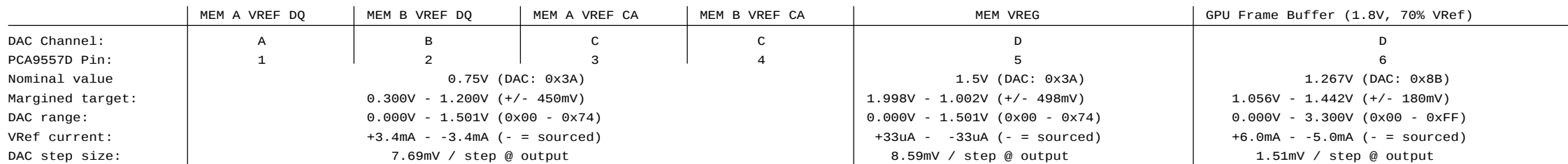
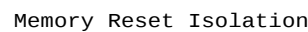
- PP3V3_S3_VREFMRGN

Signal aliases required by this page:

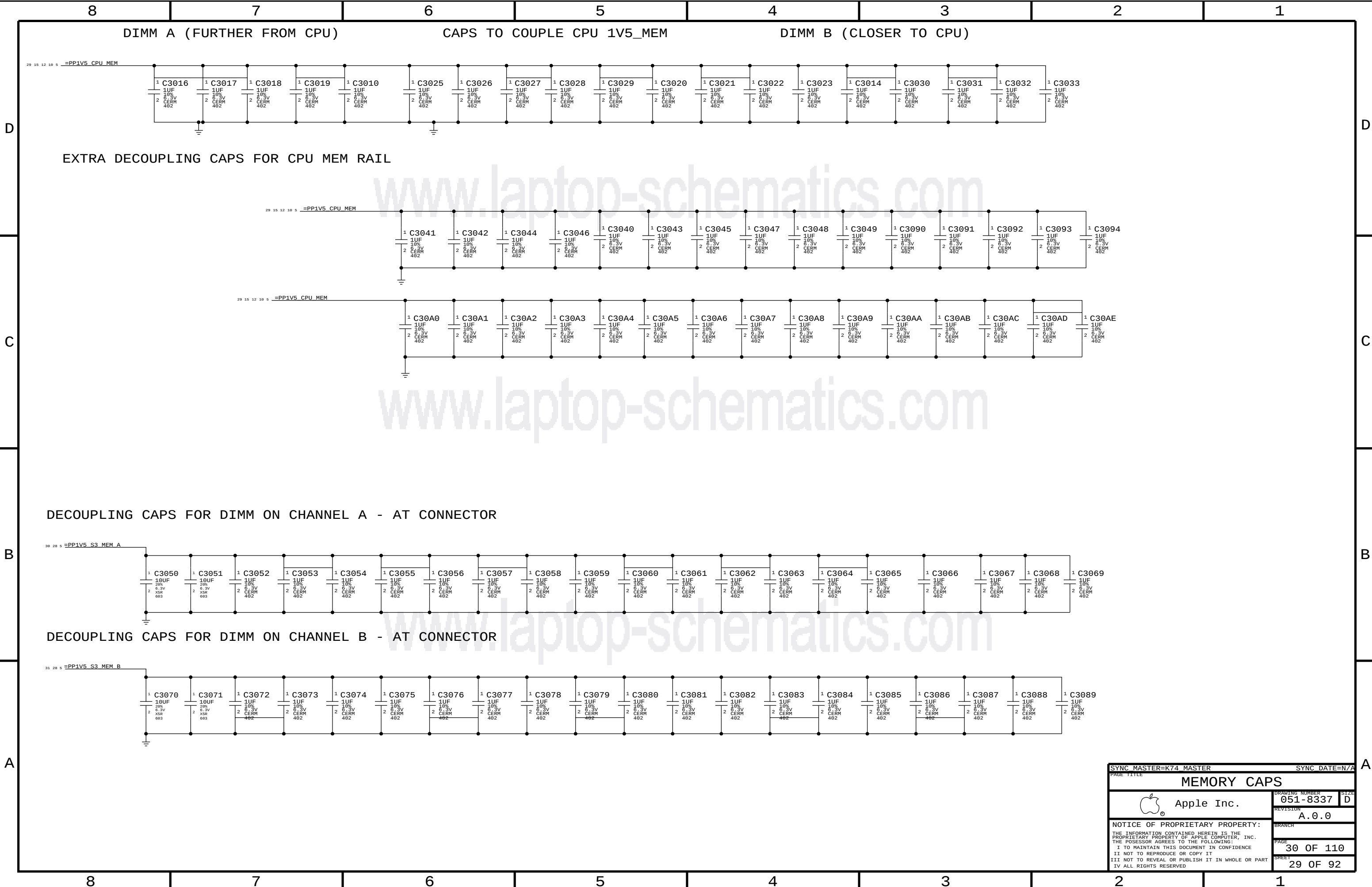
- I2C_VREFDACS_SCL
- I2C_VREFDACS_SDA
- I2C_PCA9557D_SCL
- I2C_PCA9557D_SDA

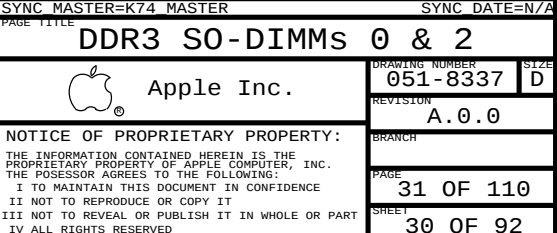
BOM options provided by this page:

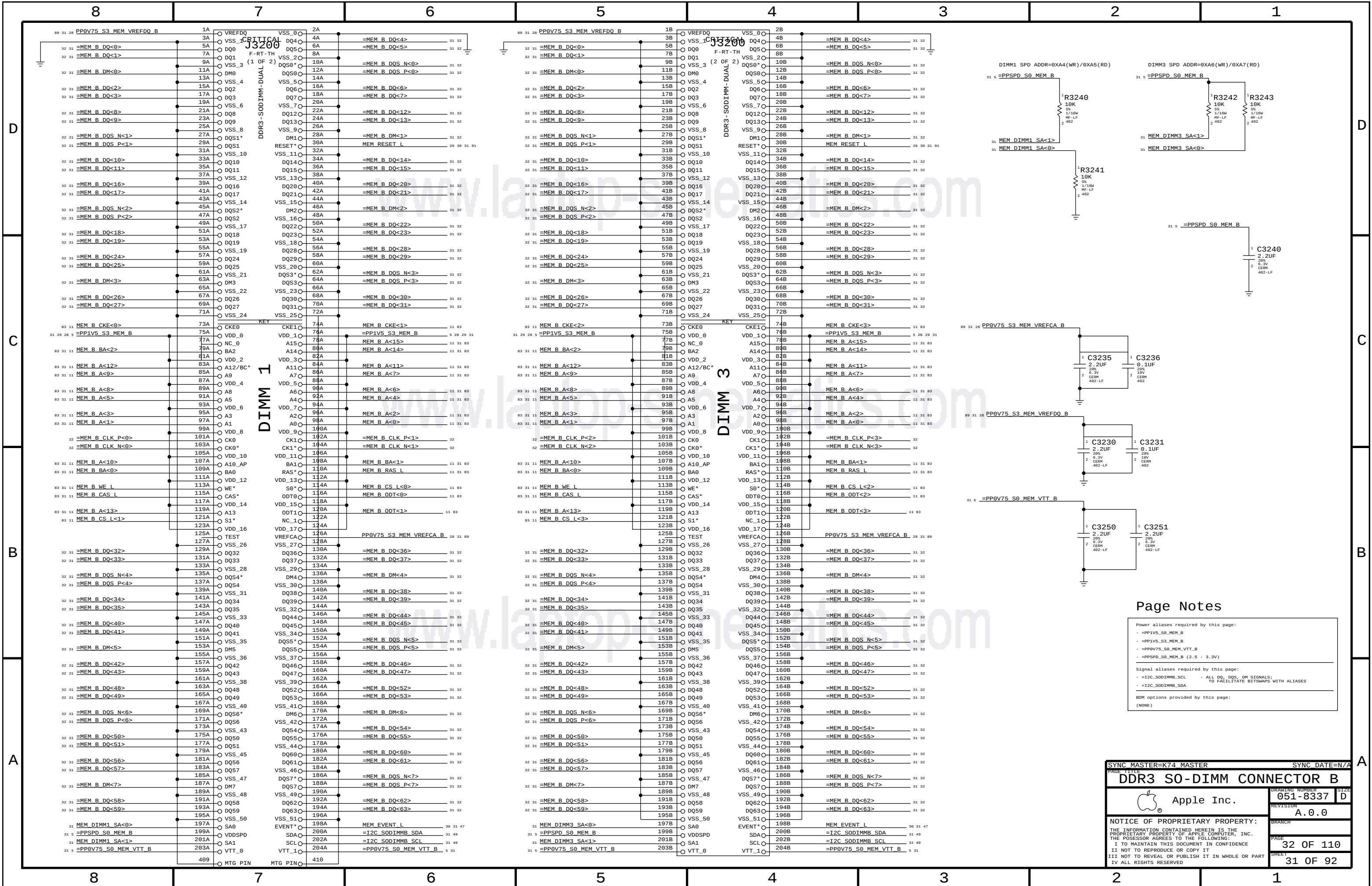
VREFMRGN - Stuffs VREF Margining Circuitry.



SYMC MASTER-MATT		SYMC DATE=01/06/2010	
PAGE TITLE			
DDR3 Vref Margining			
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		REVISION	A.0.0
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Page Notes

- Power aliases required by this page:
- PP1V5_S0_MEM_B
 - PP1V5_S3_MEM_B
 - PP0V75_S0_MEM_VTT_B
 - PPSPD_S0_MEM_B (2.5 - 3.3V)
- Signal aliases required by this page:
- I2C_S0DIMMB_SCL - ALL DQ, DQS, DM SIGNALS;
 - I2C_S0DIMMB_SDA - TO FACILITATE BITMAPS WITH ALIASES
- BOM options provided by this page:
- (NONE)

SYNC MASTER=K74 MASTER SYNC DATE=N/A

DDR3 S0-DIMM CONNECTOR B

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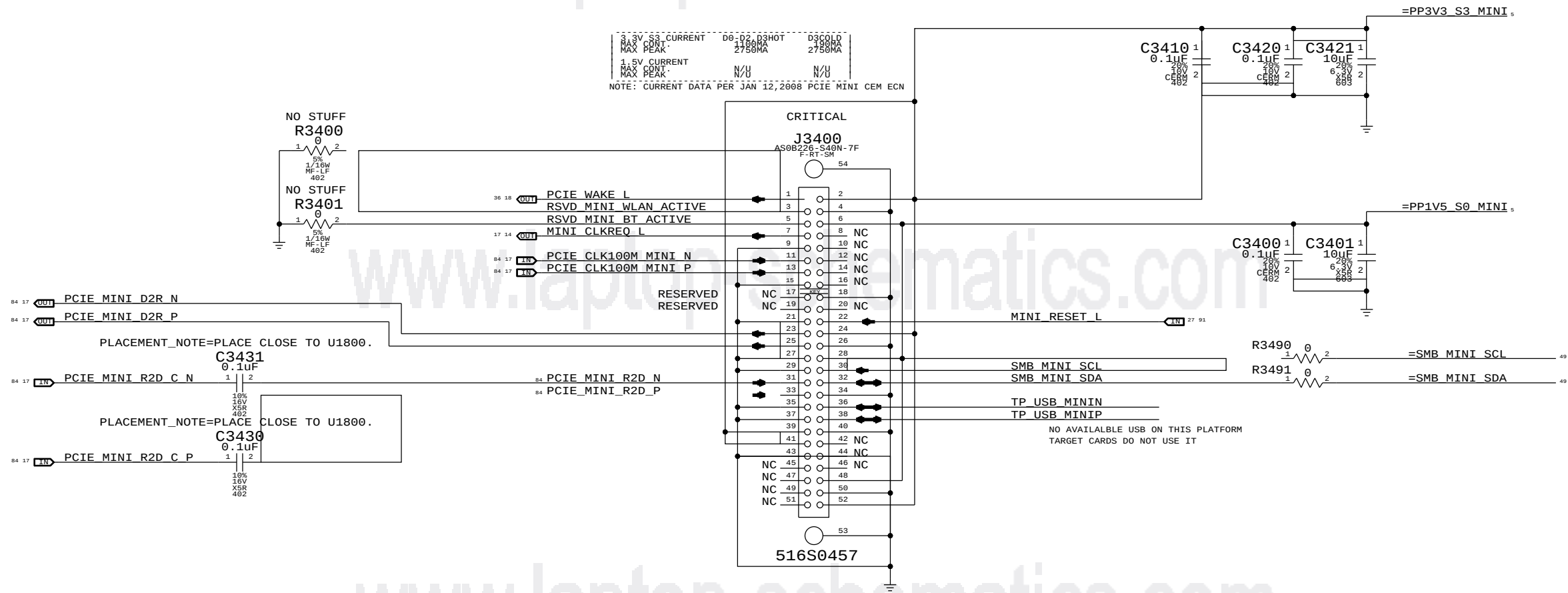
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8	7	6	5	4	3	2	1
D	CPU CHANNEL A DQS 0 -> DIMM A DQS 7		CPU CHANNEL B DQS 0 -> DIMM B DQS 7				
	MEM A DQS N<0>	=MEM A DQS N<7>	MEM B DQS N<0>	=MEM B DQS N<7>			
	MEM A DQS P<0>	MAKE_BASE=TRUE	MEM B DQS P<0>	MAKE_BASE=TRUE			
	MEM A DM<0>	MAKE_BASE=TRUE	MEM B DM<0>	MAKE_BASE=TRUE			
	MEM A DQ<7>	MAKE_BASE=TRUE	MEM B DQ<7>	MAKE_BASE=TRUE			
	MEM A DQ<6>	MAKE_BASE=TRUE	MEM B DQ<6>	MAKE_BASE=TRUE			
	MEM A DQ<5>	MAKE_BASE=TRUE	MEM B DQ<5>	MAKE_BASE=TRUE			
	MEM A DQ<4>	MAKE_BASE=TRUE	MEM B DQ<4>	MAKE_BASE=TRUE			
	MEM A DQ<3>	MAKE_BASE=TRUE	MEM B DQ<3>	MAKE_BASE=TRUE			
	MEM A DQ<2>	MAKE_BASE=TRUE	MEM B DQ<2>	MAKE_BASE=TRUE			
C	CPU CHANNEL A DQS 1 -> DIMM A DQS 6		CPU CHANNEL B DQS 1 -> DIMM B DQS 6				
	MEM A DQS N<1>	=MEM A DQS N<6>	MEM B DQS N<1>	=MEM B DQS N<6>			
	MEM A DQS P<1>	MAKE_BASE=TRUE	MEM B DQS P<1>	MAKE_BASE=TRUE			
	MEM A DM<1>	MAKE_BASE=TRUE	MEM B DM<1>	MAKE_BASE=TRUE			
	MEM A DQ<15>	MAKE_BASE=TRUE	MEM B DQ<15>	MAKE_BASE=TRUE			
	MEM A DQ<14>	MAKE_BASE=TRUE	MEM B DQ<14>	MAKE_BASE=TRUE			
	MEM A DQ<13>	MAKE_BASE=TRUE	MEM B DQ<13>	MAKE_BASE=TRUE			
	MEM A DQ<12>	MAKE_BASE=TRUE	MEM B DQ<12>	MAKE_BASE=TRUE			
	MEM A DQ<11>	MAKE_BASE=TRUE	MEM B DQ<11>	MAKE_BASE=TRUE			
	MEM A DQ<10>	MAKE_BASE=TRUE	MEM B DQ<10>	MAKE_BASE=TRUE			
B	CPU CHANNEL A DQS 2 -> DIMM A DQS 5		CPU CHANNEL B DQS 2 -> DIMM B DQS 5				
	MEM A DQS N<2>	=MEM A DQS N<5>	MEM B DQS N<2>	=MEM B DQS N<5>			
	MEM A DQS P<2>	MAKE_BASE=TRUE	MEM B DQS P<2>	MAKE_BASE=TRUE			
	MEM A DM<2>	MAKE_BASE=TRUE	MEM B DM<2>	MAKE_BASE=TRUE			
	MEM A DQ<23>	MAKE_BASE=TRUE	MEM B DQ<23>	MAKE_BASE=TRUE			
	MEM A DQ<22>	MAKE_BASE=TRUE	MEM B DQ<22>	MAKE_BASE=TRUE			
	MEM A DQ<21>	MAKE_BASE=TRUE	MEM B DQ<21>	MAKE_BASE=TRUE			
	MEM A DQ<20>	MAKE_BASE=TRUE	MEM B DQ<20>	MAKE_BASE=TRUE			
	MEM A DQ<19>	MAKE_BASE=TRUE	MEM B DQ<19>	MAKE_BASE=TRUE			
	MEM A DQ<18>	MAKE_BASE=TRUE	MEM B DQ<18>	MAKE_BASE=TRUE			
A	CPU CHANNEL A DQS 3 -> DIMM A DQS 4		CPU CHANNEL B DQS 3 -> DIMM B DQS 4				
	MEM A DQS N<3>	=MEM A DQS N<4>	MEM B DQS N<3>	=MEM B DQS N<4>			
	MEM A DQS P<3>	MAKE_BASE=TRUE	MEM B DQS P<3>	MAKE_BASE=TRUE			
	MEM A DM<3>	MAKE_BASE=TRUE	MEM B DM<3>	MAKE_BASE=TRUE			
	MEM A DQ<31>	MAKE_BASE=TRUE	MEM B DQ<31>	MAKE_BASE=TRUE			
	MEM A DQ<30>	MAKE_BASE=TRUE	MEM B DQ<30>	MAKE_BASE=TRUE			
	MEM A DQ<29>	MAKE_BASE=TRUE	MEM B DQ<29>	MAKE_BASE=TRUE			
	MEM A DQ<28>	MAKE_BASE=TRUE	MEM B DQ<28>	MAKE_BASE=TRUE			
	MEM A DQ<27>	MAKE_BASE=TRUE	MEM B DQ<27>	MAKE_BASE=TRUE			
	MEM A DQ<26>	MAKE_BASE=TRUE	MEM B DQ<26>	MAKE_BASE=TRUE			
A	CPU CHANNEL A DQS 4 -> DIMM A DQS 3		CPU CHANNEL B DQS 4 -> DIMM B DQS 3				
	MEM A DQS N<4>	=MEM A DQS N<3>	MEM B DQS N<4>	=MEM B DQS N<3>			
	MEM A DQS P<4>	MAKE_BASE=TRUE	MEM B DQS P<4>	MAKE_BASE=TRUE			
	MEM A DM<4>	MAKE_BASE=TRUE	MEM B DM<4>	MAKE_BASE=TRUE			
	MEM A DQ<39>	MAKE_BASE=TRUE	MEM B DQ<39>	MAKE_BASE=TRUE			
	MEM A DQ<38>	MAKE_BASE=TRUE	MEM B DQ<38>	MAKE_BASE=TRUE			
	MEM A DQ<37>	MAKE_BASE=TRUE	MEM B DQ<37>	MAKE_BASE=TRUE			
	MEM A DQ<36>	MAKE_BASE=TRUE	MEM B DQ<36>	MAKE_BASE=TRUE			
	MEM A DQ<35>	MAKE_BASE=TRUE	MEM B DQ<35>	MAKE_BASE=TRUE			
	MEM A DQ<34>	MAKE_BASE=TRUE	MEM B DQ<34>	MAKE_BASE=TRUE			
A	CPU CHANNEL A DQS 5 -> DIMM A DQS 2		CPU CHANNEL B DQS 5 -> DIMM B DQS 2				
	MEM A DQS N<5>	=MEM A DQS N<2>	MEM B DQS N<5>	=MEM B DQS N<2>			
	MEM A DQS P<5>	MAKE_BASE=TRUE	MEM B DQS P<5>	MAKE_BASE=TRUE			
	MEM A DM<5>	MAKE_BASE=TRUE	MEM B DM<5>	MAKE_BASE=TRUE			
	MEM A DQ<47>	MAKE_BASE=TRUE	MEM B DQ<47>	MAKE_BASE=TRUE			
	MEM A DQ<46>	MAKE_BASE=TRUE	MEM B DQ<46>	MAKE_BASE=TRUE			
	MEM A DQ<45>	MAKE_BASE=TRUE	MEM B DQ<45>	MAKE_BASE=TRUE			
	MEM A DQ<44>	MAKE_BASE=TRUE	MEM B DQ<44>	MAKE_BASE=TRUE			
	MEM A DQ<43>	MAKE_BASE=TRUE	MEM B DQ<43>	MAKE_BASE=TRUE			
	MEM A DQ<42>	MAKE_BASE=TRUE	MEM B DQ<42>	MAKE_BASE=TRUE			
A	CPU CHANNEL A DQS 6 -> DIMM A DQS 1		CPU CHANNEL B DQS 6 -> DIMM B DQS 1				
	MEM A DQS N<6>	=MEM A DQS N<1>	MEM B DQS N<6>	=MEM B DQS N<1>			
	MEM A DQS P<6>	MAKE_BASE=TRUE	MEM B DQS P<6>	MAKE_BASE=TRUE			
	MEM A DM<6>	MAKE_BASE=TRUE	MEM B DM<6>	MAKE_BASE=TRUE			
	MEM A DQ<55>	MAKE_BASE=TRUE	MEM B DQ<55>	MAKE_BASE=TRUE			
	MEM A DQ<54>	MAKE_BASE=TRUE	MEM B DQ<54>	MAKE_BASE=TRUE			
	MEM A DQ<53>	MAKE_BASE=TRUE	MEM B DQ<53>	MAKE_BASE=TRUE			
	MEM A DQ<52>	MAKE_BASE=TRUE	MEM B DQ<52>	MAKE_BASE=TRUE			
	MEM A DQ<51>	MAKE_BASE=TRUE	MEM B DQ<51>	MAKE_BASE=TRUE			
	MEM A DQ<50>	MAKE_BASE=TRUE	MEM B DQ<50>	MAKE_BASE=TRUE			
A	CPU CHANNEL A DQS 7 -> DIMM A DQS 0		CPU CHANNEL B DQS 7 -> DIMM B DQS 0				
	MEM A DQS N<7>	=MEM A DQS N<0>	MEM B DQS N<7>	=MEM B DQS N<0>			
	MEM A DQS P<7>	MAKE_BASE=TRUE	MEM B DQS P<7>	MAKE_BASE=TRUE			
	MEM A DM<7>	MAKE_BASE=TRUE	MEM B DM<7>	MAKE_BASE=TRUE			
	MEM A DQ<63>	MAKE_BASE=TRUE	MEM B DQ<63>	MAKE_BASE=TRUE			
	MEM A DQ<62>	MAKE_BASE=TRUE	MEM B DQ<62>	MAKE_BASE=TRUE			
	MEM A DQ<61>	MAKE_BASE=TRUE	MEM B DQ<61>	MAKE_BASE=TRUE			
	MEM A DQ<60>	MAKE_BASE=TRUE	MEM B DQ<60>	MAKE_BASE=TRUE			
	MEM A DQ<59>	MAKE_BASE=TRUE	MEM B DQ<59>	MAKE_BASE=TRUE			
	MEM A DQ<58>	MAKE_BASE=TRUE	MEM B DQ<58>	MAKE_BASE=TRUE			
MEMORY CLOCK ALIASING							
MEM A CLK P<0>	MAKE_BASE=TRUE	=MEM A CLK P<0>	MEM B CLK P<0>	MAKE_BASE=TRUE	=MEM B CLK P<0>		
MEM A CLK N<0>	MAKE_BASE=TRUE	=MEM A CLK N<0>	MEM B CLK N<0>	MAKE_BASE=TRUE	=MEM B CLK N<0>		
MEM A CLK P<1>	MAKE_BASE=TRUE	=MEM A CLK P<1>	MEM B CLK P<1>	MAKE_BASE=TRUE	=MEM B CLK P<1>		
MEM A CLK N<1>	MAKE_BASE=TRUE	=MEM A CLK N<1>	MEM B CLK N<1>	MAKE_BASE=TRUE	=MEM B CLK N<1>		
MEM A CLK P<2>	MAKE_BASE=TRUE	=MEM A CLK P<2>	MEM B CLK P<2>	MAKE_BASE=TRUE	=MEM B CLK P<2>		
MEM A CLK N<2>	MAKE_BASE=TRUE	=MEM A CLK N<2>	MEM B CLK N<2>	MAKE_BASE=TRUE	=MEM B CLK N<2>		
MEM A CLK P<3>	MAKE_BASE=TRUE	=MEM A CLK P<3>	MEM B CLK P<3>	MAKE_BASE=TRUE	=MEM B CLK P<3>		
MEM A CLK N<3>	MAKE_BASE=TRUE	=MEM A CLK N<3>	MEM B CLK N<3>	MAKE_BASE=TRUE	=MEM B CLK N<3>		
SYNC MASTER=K74 MASTER SYNC DATE=N/A DDR3 ALIAS AND BITSWAPS Apple Inc. NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED							
8	7	6	5	4	3	2	1

SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE			
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Apple Inc.		DRAWING NUMBER	051-8337
		REVISION	A.0.0
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PAGE		33 OF 110	
SHEET		32 OF 92	

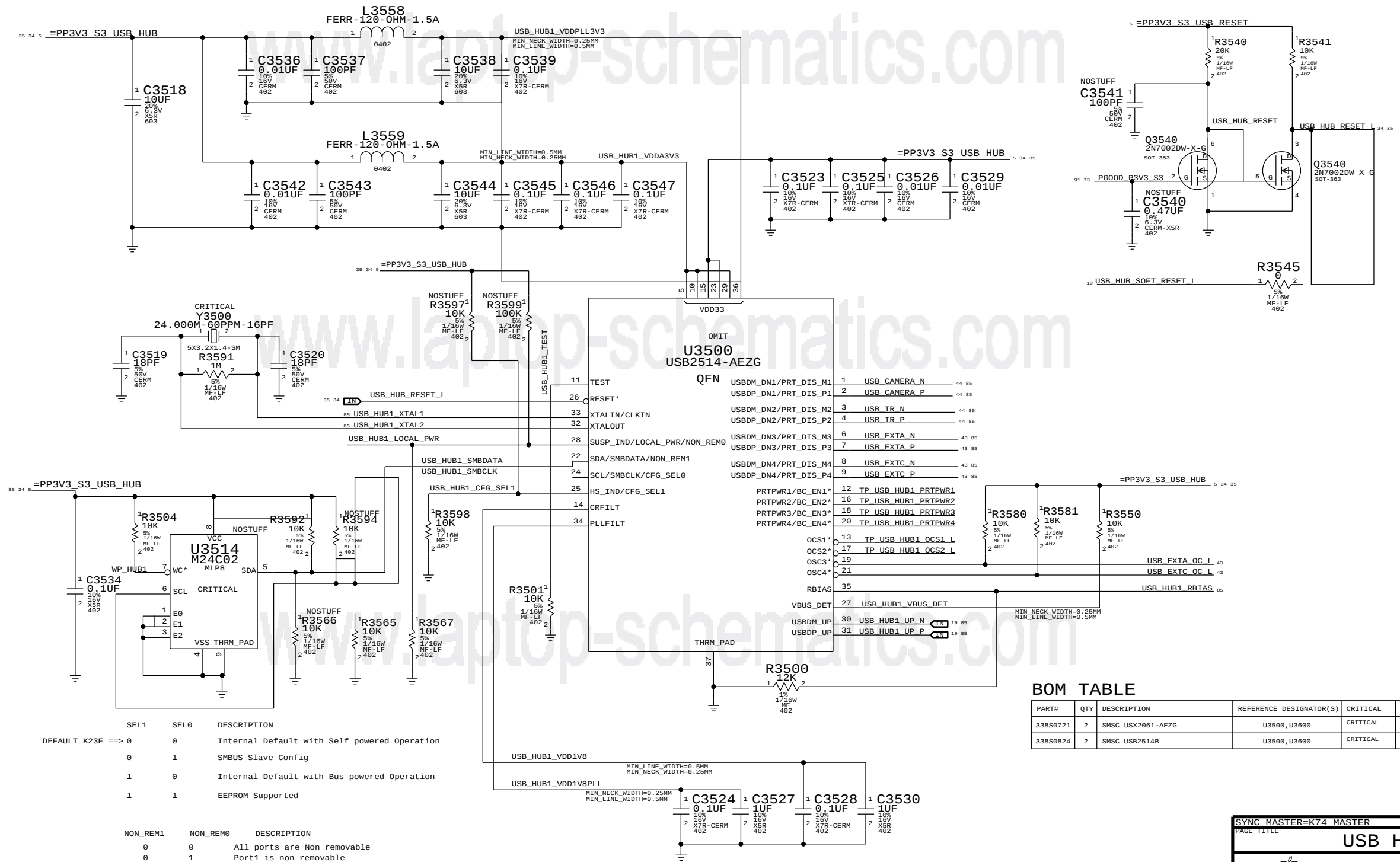
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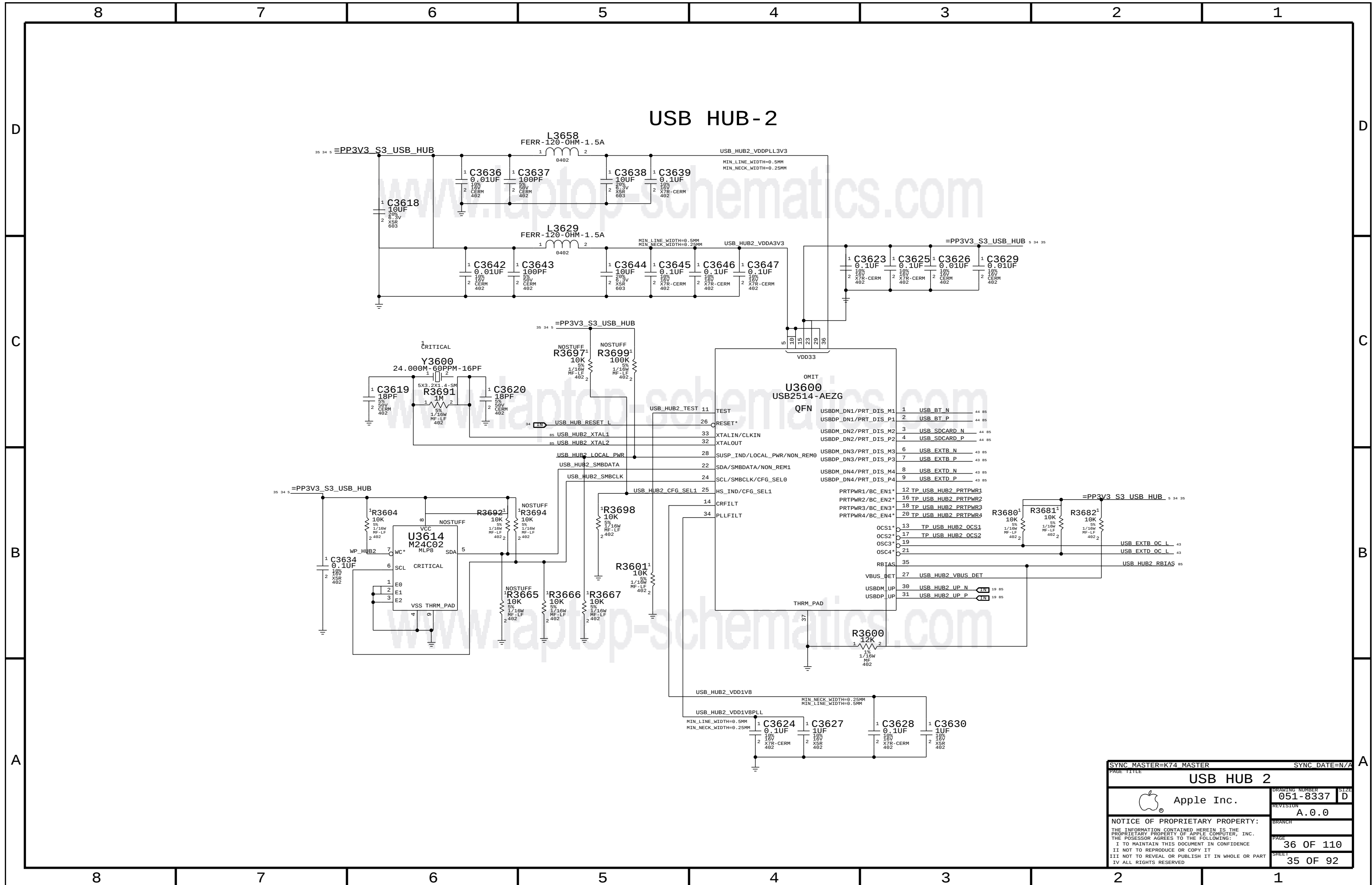
SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE 0011			
PCI-E MiniCard Connector			
 Apple Inc.		DRAWING NUMBER	051-8337
		SIZE	D
		REVISION	A.0.0
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USB HUB-1



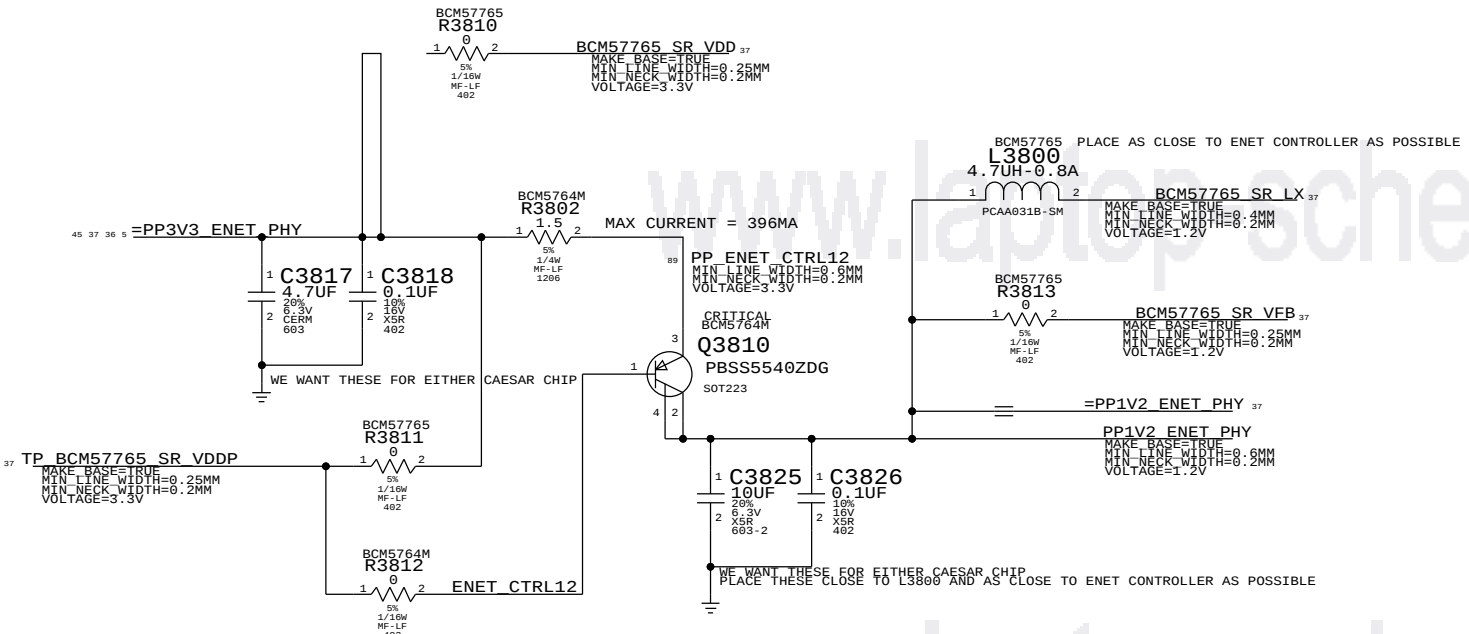
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0721	2	SMSC USX2061-AEZ6	U3500, U3600	CRITICAL	HUB_USX2061
338S0824	2	SMSC USB2514B	U3500, U3600	CRITICAL	HUB_USB2514B

SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE			
USB HUB 1			
 Apple Inc.		DRAWING NUMBER 051-8337	
		SIZE D	
		REVISION A.0.0	
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		SHEET 34 OF 92	

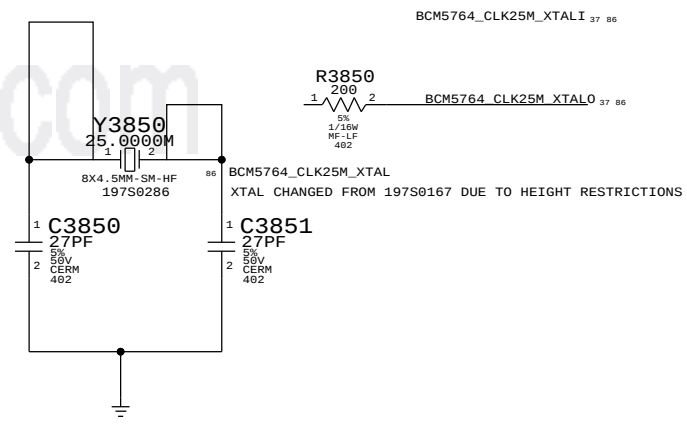


SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE			
USB HUB 2			
 Apple Inc.		DRAWING NUMBER	051-8337
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		PAGE	36 OF 110
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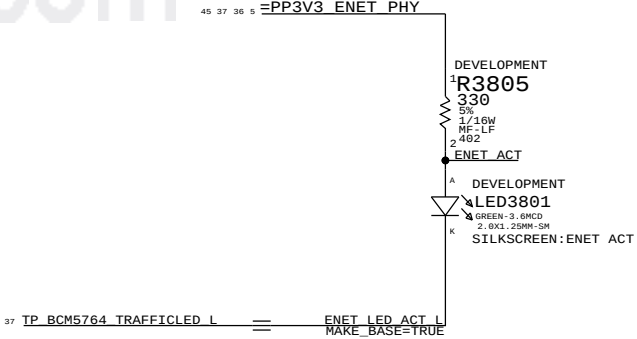
CAESAR II/IV 1V2 RAIL SUPPLY



CAESAR II/IV 25MHZ XTAL

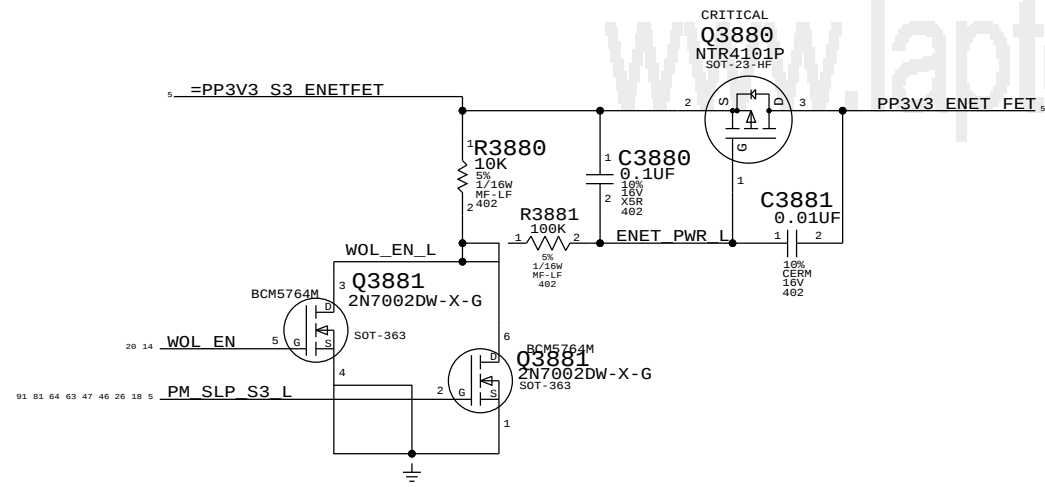


CAESAR II/IV ACTIVITY LED

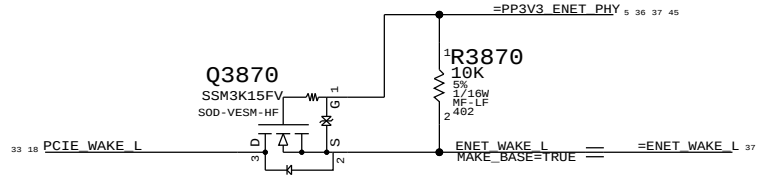


3.3V ENET FET

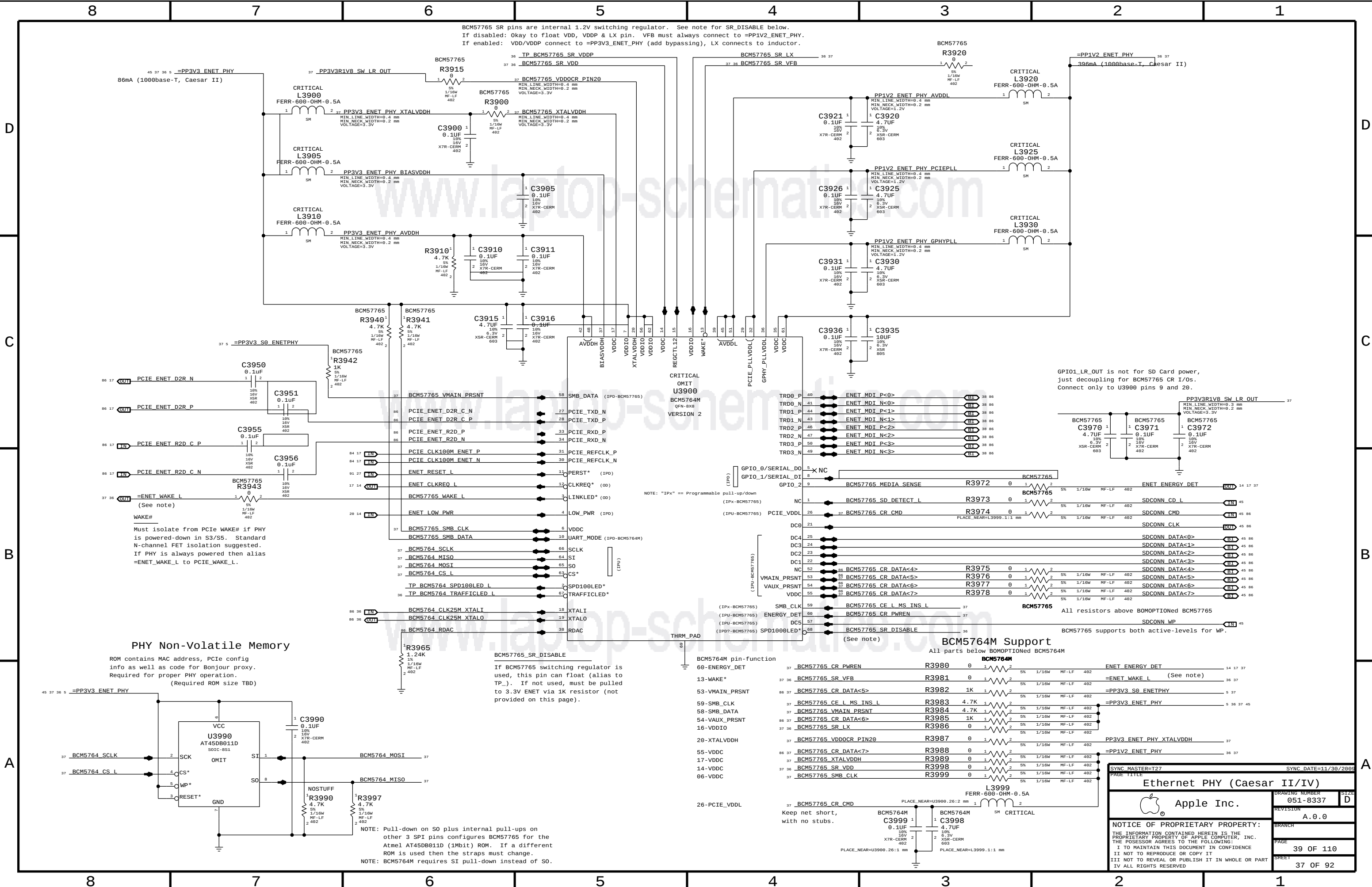
ENET_PWR_ON = "S0" || (S3 power && WOL_EN)



CAESAR II/IV WAKE# ISOLATION

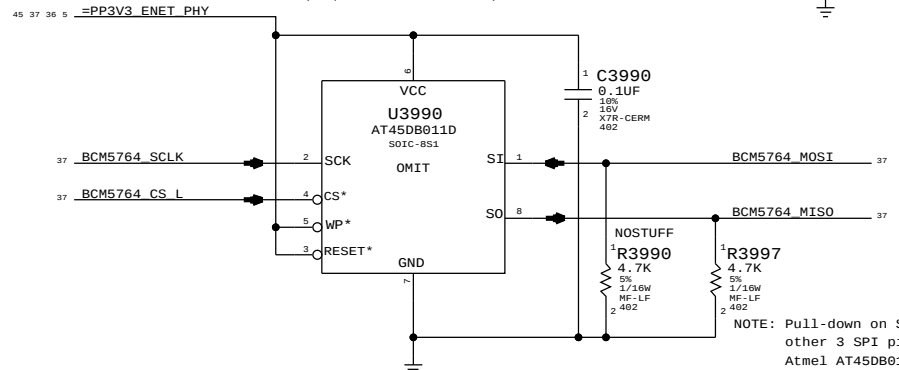


SYNC MASTER=MASTER		SYNC DATE=N/A	
PAGE TITLE		Caesar II/IV Support	
Apple Inc.		DRAWING NUMBER	051-8337
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PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation. (Required ROM size TBD)



BCM57765_SR_DISABLE

If BCM57765 switching regulator is used, this pin can float (alias to TP...). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

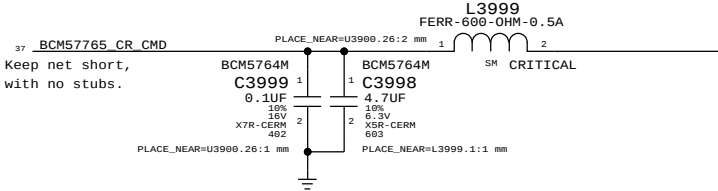
BCM5764M pin-function

- 60-ENERGY_DET
- 13-WAKE*
- 53-VMAIN_PRSN
- 59-SMB_CLK
- 58-SMB_DATA
- 54-VAUX_PRSN
- 16-VDDIO
- 20-XTALVDDH
- 55-VDDC
- 17-VDDC
- 14-VDDC
- 96-VDDC
- 26-PCIE_VDDL

BCM5764M Support

All parts below BOMOPTIONed BCM5764M

37 BCM57765 CR PWREN	R3980	0	1	5%	1/16W	MF-LF	402	ENET ENERGY_DET	14 17 37
37 BCM57765 SR VFB	R3981	0	1	5%	1/16W	MF-LF	402	=ENET_WAKE_L (See note)	36 37
37 BCM57765 CR DATA<5>	R3982	1K	1	5%	1/16W	MF-LF	402	=PP3V3 S0 ENETPHY	5 37
37 BCM57765 CE L MS INS L	R3983	4.7K	1	5%	1/16W	MF-LF	402	=PP3V3 ENET PHY	5 36 37 45
37 BCM57765 VMAIN_PRSN	R3984	4.7K	1	5%	1/16W	MF-LF	402		
37 BCM57765 CR DATA<6>	R3985	1K	1	5%	1/16W	MF-LF	402		
37 BCM57765 SR LX	R3986	0	1	5%	1/16W	MF-LF	402		
37 BCM57765 VDDOCR_PIN20	R3987	0	1	5%	1/16W	MF-LF	402	PP3V3 ENET PHY XTALVDDH	37
37 BCM57765 CR DATA<7>	R3988	0	1	5%	1/16W	MF-LF	402		
37 BCM57765 XTALVDDH	R3989	0	1	5%	1/16W	MF-LF	402	=PP1V2 ENET PHY	36 37
37 BCM57765 SR VDD	R3990	0	1	5%	1/16W	MF-LF	402		
37 BCM57765 SMB_CLK	R3999	0	1	5%	1/16W	MF-LF	402		



SYNC MASTER=T27

SYNC DATE=11/30/2008

Ethernet PHY (Caesar II/IV)

Apple Inc.

051-8337

A.0.0

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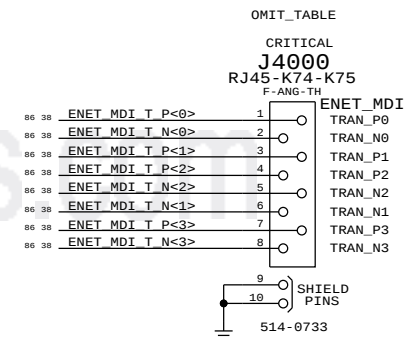
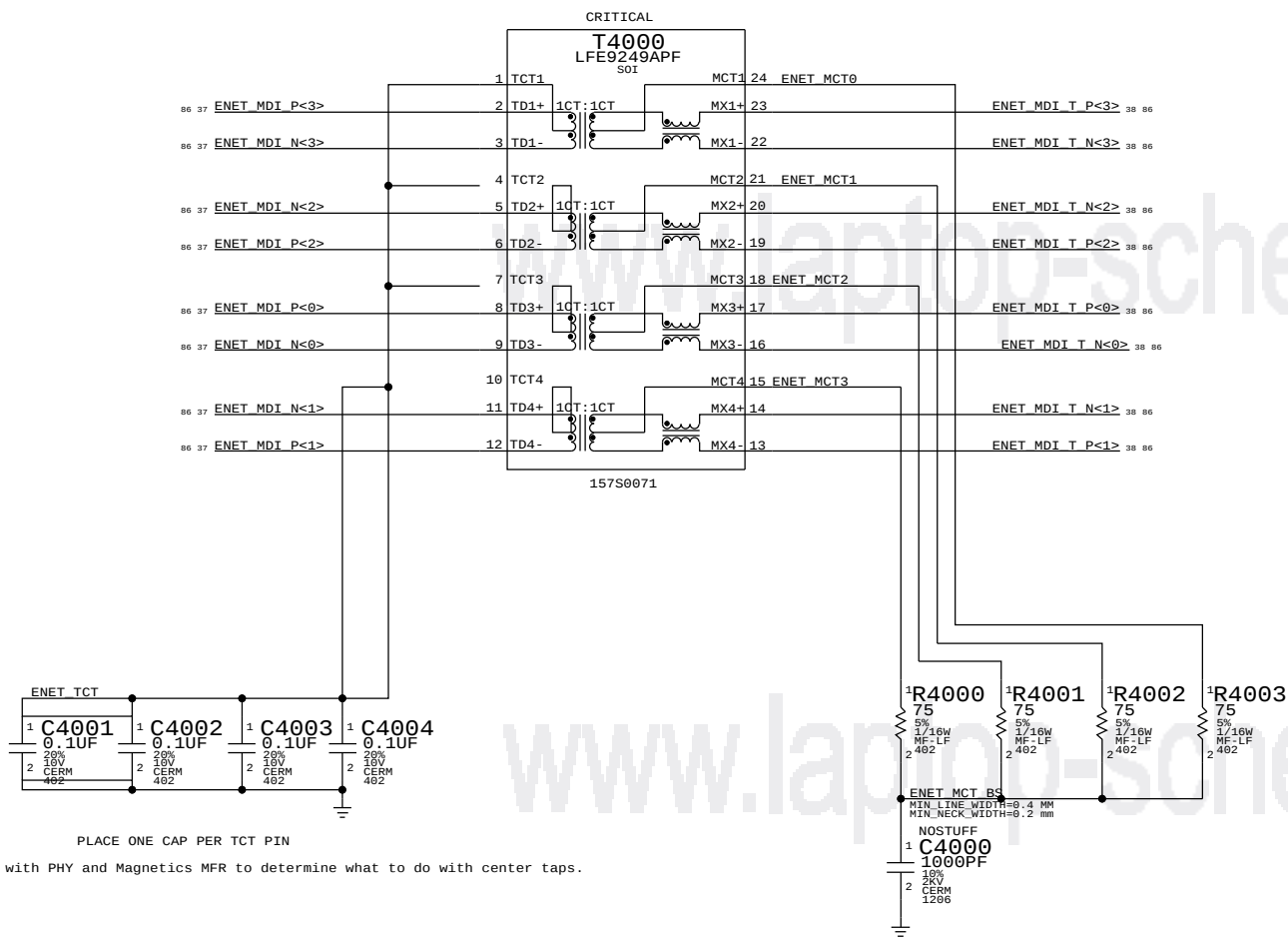
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37 OF 92

NOTE: Pull-down on S0 plus internal pull-ups on other 3 SPI pins configures BCM57765 for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.

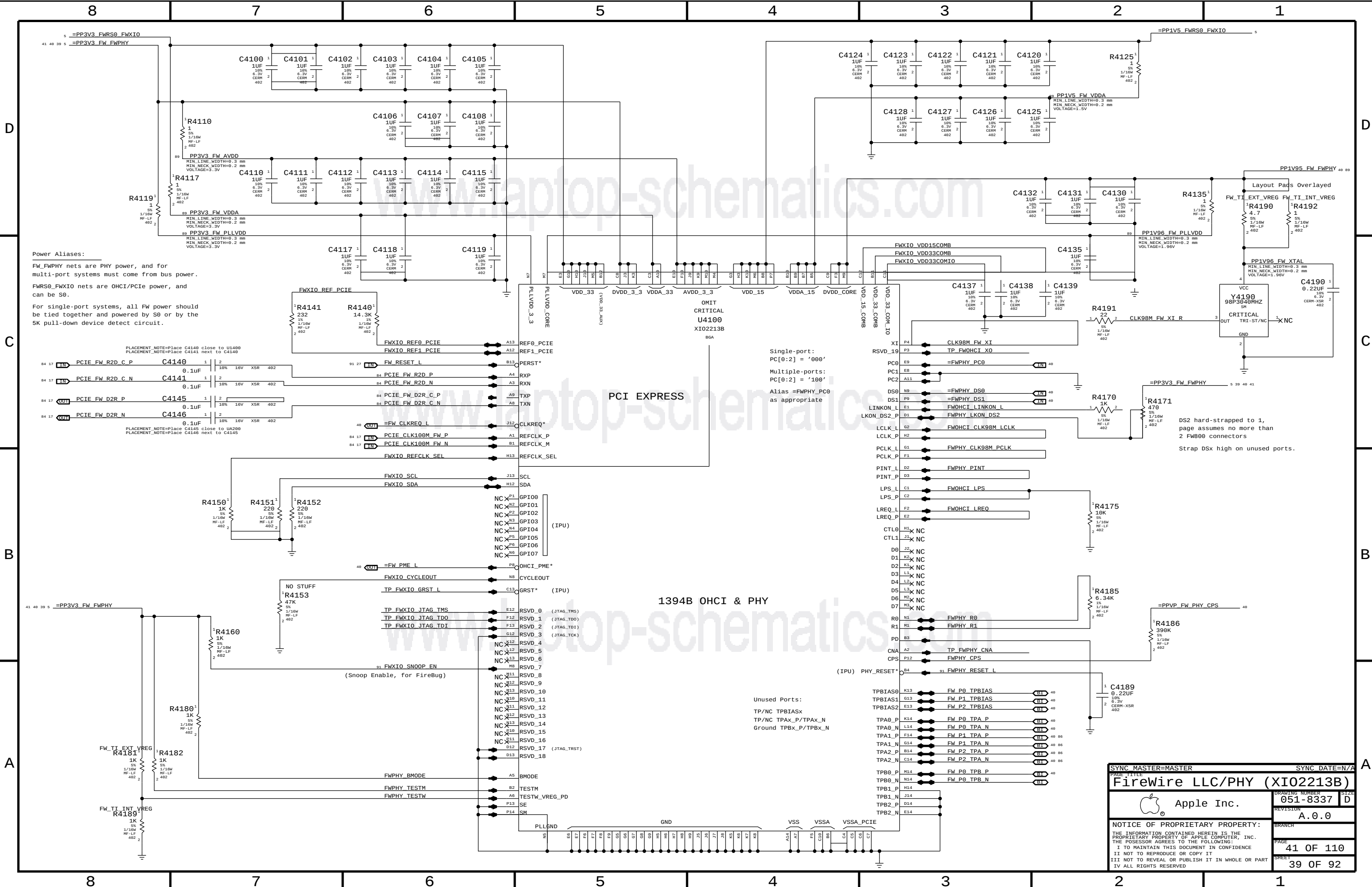
NOTE: BCM5764M requires SI pull-down instead of S0.

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0654	1	K22/K23 PROD. RJ45	J4000	CRITICAL	METAL_IO
514-0733	1	K74/K75 RJ45, PLASTIC, PD/NI	J4000	CRITICAL	PLASTIC_IO

SYNC MASTER=MASTER		SYNC DATE=N/A	
PAGE TITLE			
Ethernet Connector			
 Apple Inc.		DRAWING NUMBER	051-8337
		SIZE	D
		REVISION	A.0.0
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		PAGE	40 OF 110
		SHEET	38 OF 92



Power Aliases:
FW_FWPHY nets are PHY power, and for multi-port systems must come from bus power.
FWRS0_FWXIO nets are OHCI/PCIE power, and can be S0.
For single-port systems, all FW power should be tied together and powered by S0 or by the 5K pull-down device detect circuit.

PLACEMENT_NOTE=Place C4140 close to U1400
PLACEMENT_NOTE=Place C4141 next to C4140
PLACEMENT_NOTE=Place C4145 close to UA200
PLACEMENT_NOTE=Place C4146 next to C4145

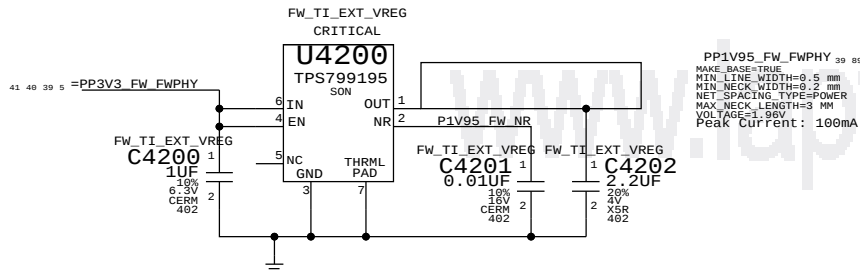
Single-port:
PC[0:2] = '000'
Multiple-ports:
PC[0:2] = '100'
Alias =FWPHY_PC0
as appropriate

DS2 hard-strapped to 1,
page assumes no more than
2 FW000 connectors
Strap DSx high on unused ports.

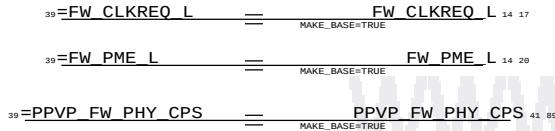
Unused Ports:
TP/NC TPBIASx
TP/NC TPAX_P/TPAX_N
Ground TPBX_P/TPBX_N

SYNC MASTER=MASTER		SYNC DATE=N/A	
PAGE TITLE		FireWire LLC/PHY (XIO2213B)	
Apple Inc.		DRAWING NUMBER	051-8337
		REVISION	A.0.0
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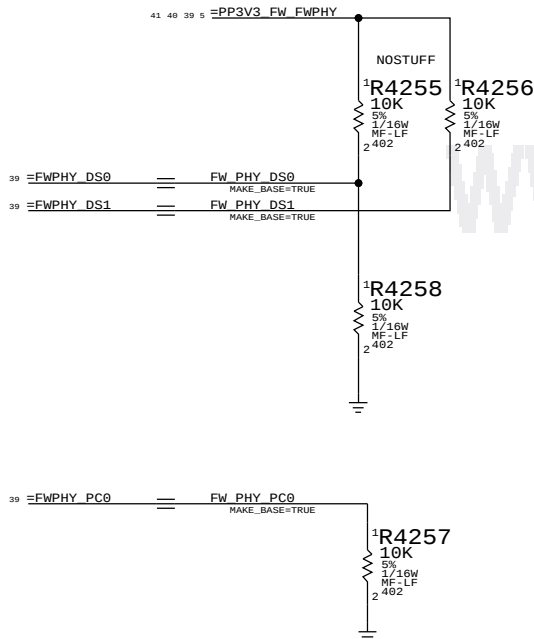
1394 PHY 1.95V SUPPLY



FireWire Aliases For Connectivity



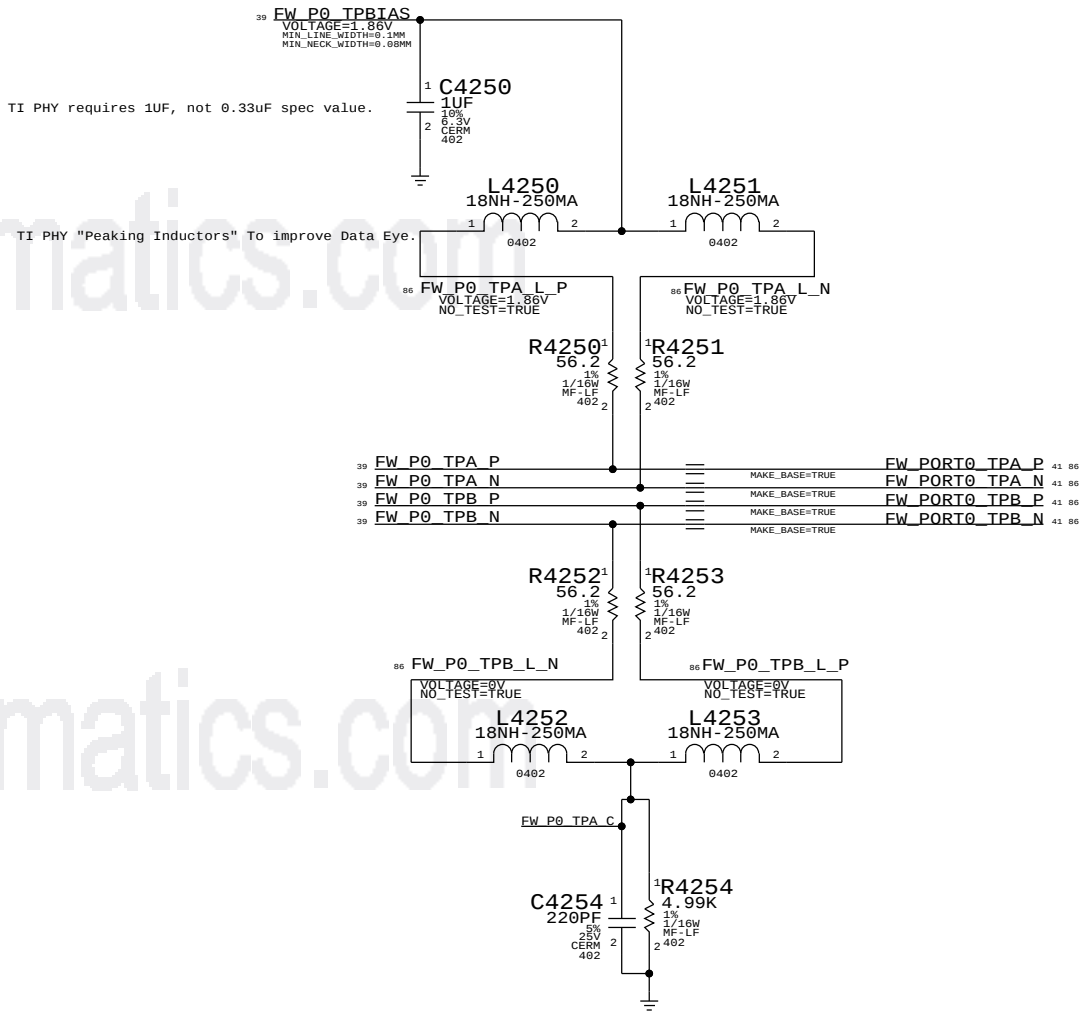
1394 PHY STRAPPING OPTIONS



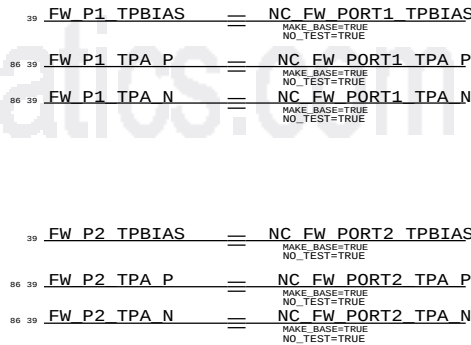
THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

iMacs are now one port only and have Power Code "000"

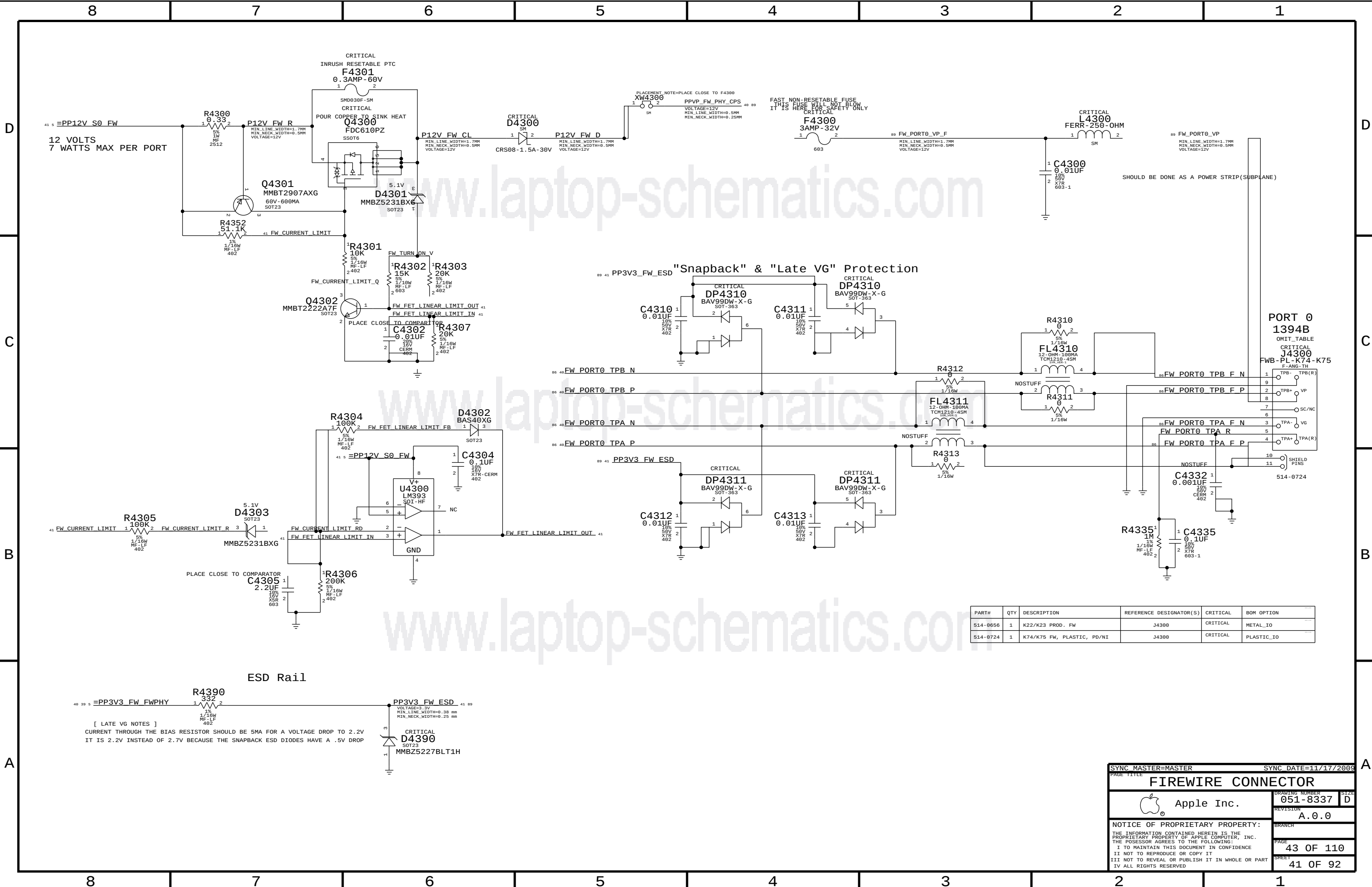
Termination
Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED



SYNC MASTER=MASTER		SYNC DATE=N/A	
PAGE TITLE		FW: 1394B MISC	
DRAWING NUMBER		051-8337	D
REVISION		A.0.0	
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0656	1	K22/K23 PROD. FW	J4300	CRITICAL	METAL_IO
514-0724	1	K74/K75 FW, PLASTIC, PD/NI	J4300	CRITICAL	PLASTIC_IO

SYNC MASTER=MASTER

SYNC DATE=11/17/2009

FIREWIRE CONNECTOR

Apple Inc.

051-8337

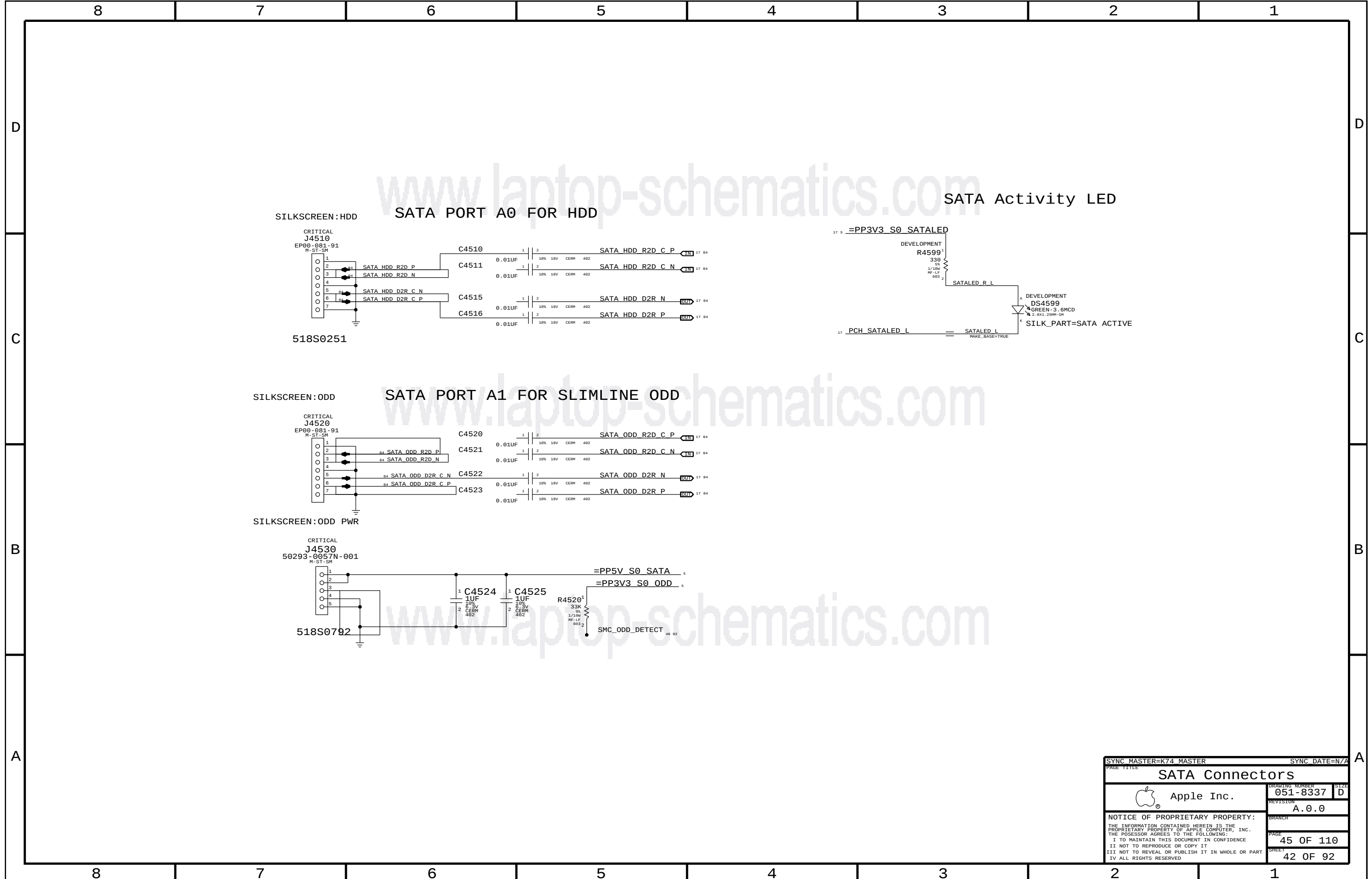
A.0.0

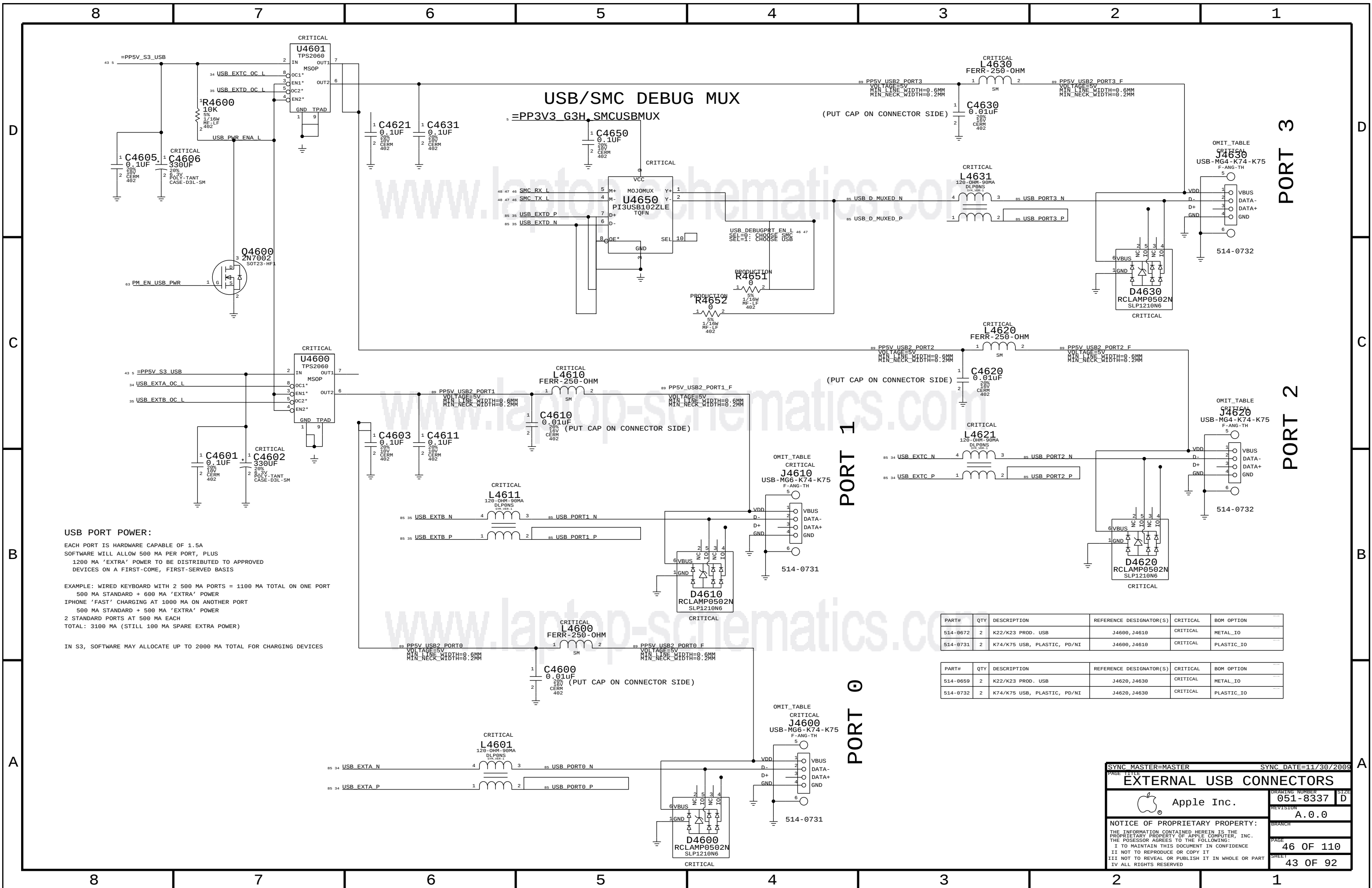
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USB PORT POWER:

EACH PORT IS HARDWARE CAPABLE OF 1.5A
SOFTWARE WILL ALLOW 500 MA PER PORT, PLUS
1200 MA 'EXTRA' POWER TO BE DISTRIBUTED TO APPROVED
DEVICES ON A FIRST-COME, FIRST-SERVED BASIS

EXAMPLE: WIRED KEYBOARD WITH 2 500 MA PORTS = 1100 MA TOTAL ON ONE PORT

500 MA STANDARD + 600 MA 'EXTRA' POWER

IPHONE 'FAST' CHARGING AT 1000 MA ON ANOTHER PORT

500 MA STANDARD + 500 MA 'EXTRA' POWER

2 STANDARD PORTS AT 500 MA EACH

TOTAL: 3100 MA (STILL 100 MA SPARE EXTRA POWER)

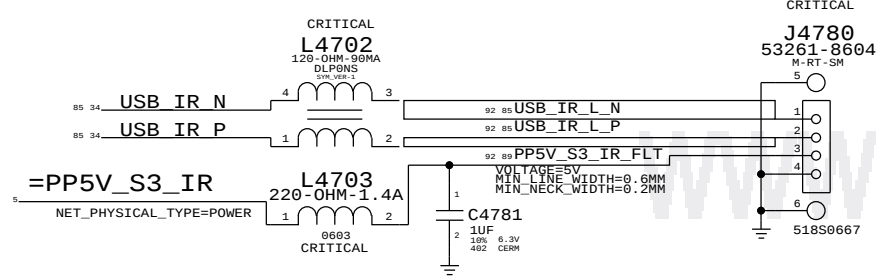
IN S3, SOFTWARE MAY ALLOCATE UP TO 2000 MA TOTAL FOR CHARGING DEVICES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
S14-0672	2	K22/K23 PROD. USB	J4600, J4610	CRITICAL	METAL_IO
S14-0731	2	K74/K75 USB, PLASTIC, PD/NI	J4600, J4610	CRITICAL	PLASTIC_IO

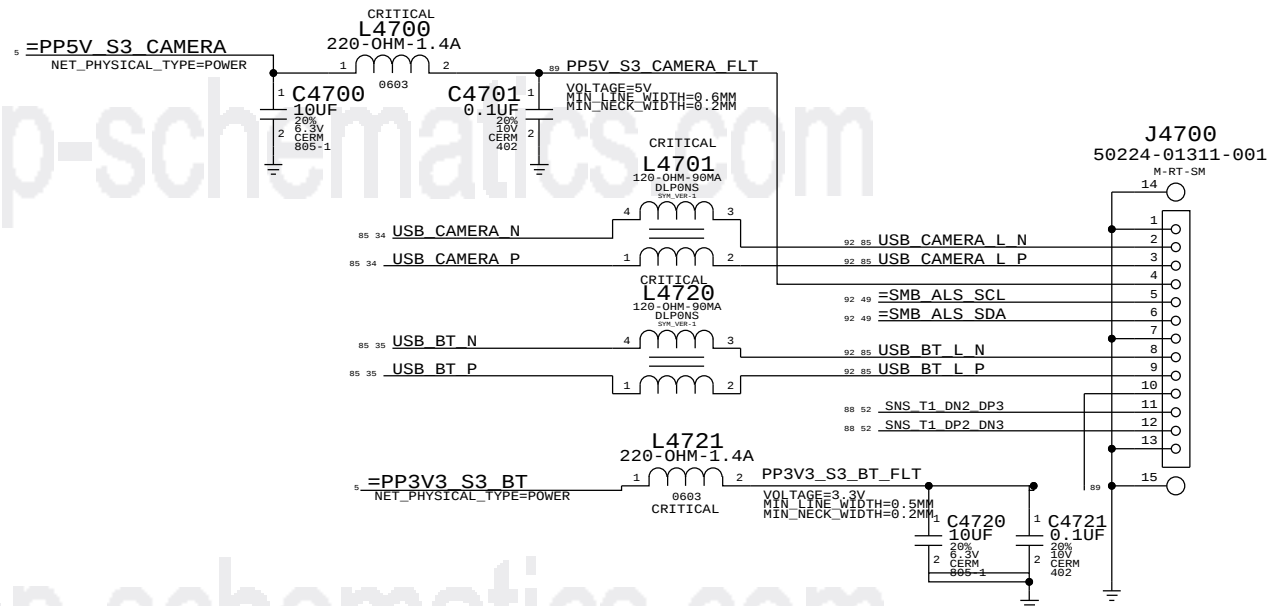
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
S14-0659	2	K22/K23 PROD. USB	J4620, J4630	CRITICAL	METAL_IO
S14-0732	2	K74/K75 USB, PLASTIC, PD/NI	J4620, J4630	CRITICAL	PLASTIC_IO

SYNC MASTER=MASTER		SYNC DATE=11/30/2009	
PAGE TITLE		EXTERNAL USB CONNECTORS	
Apple Inc.		DRAWING NUMBER	051-8337
		REVISION	A.0.0
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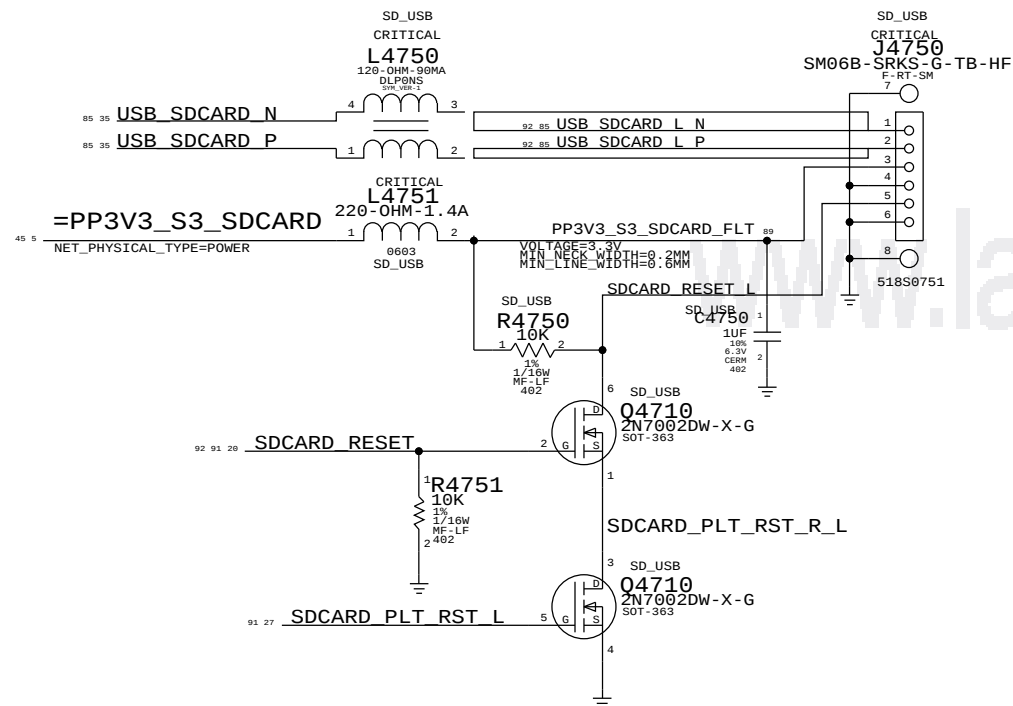
IR RECEIVER CONNECTOR



CAMERA/ALS & BLUETOOTH (K37A) CONNECTOR

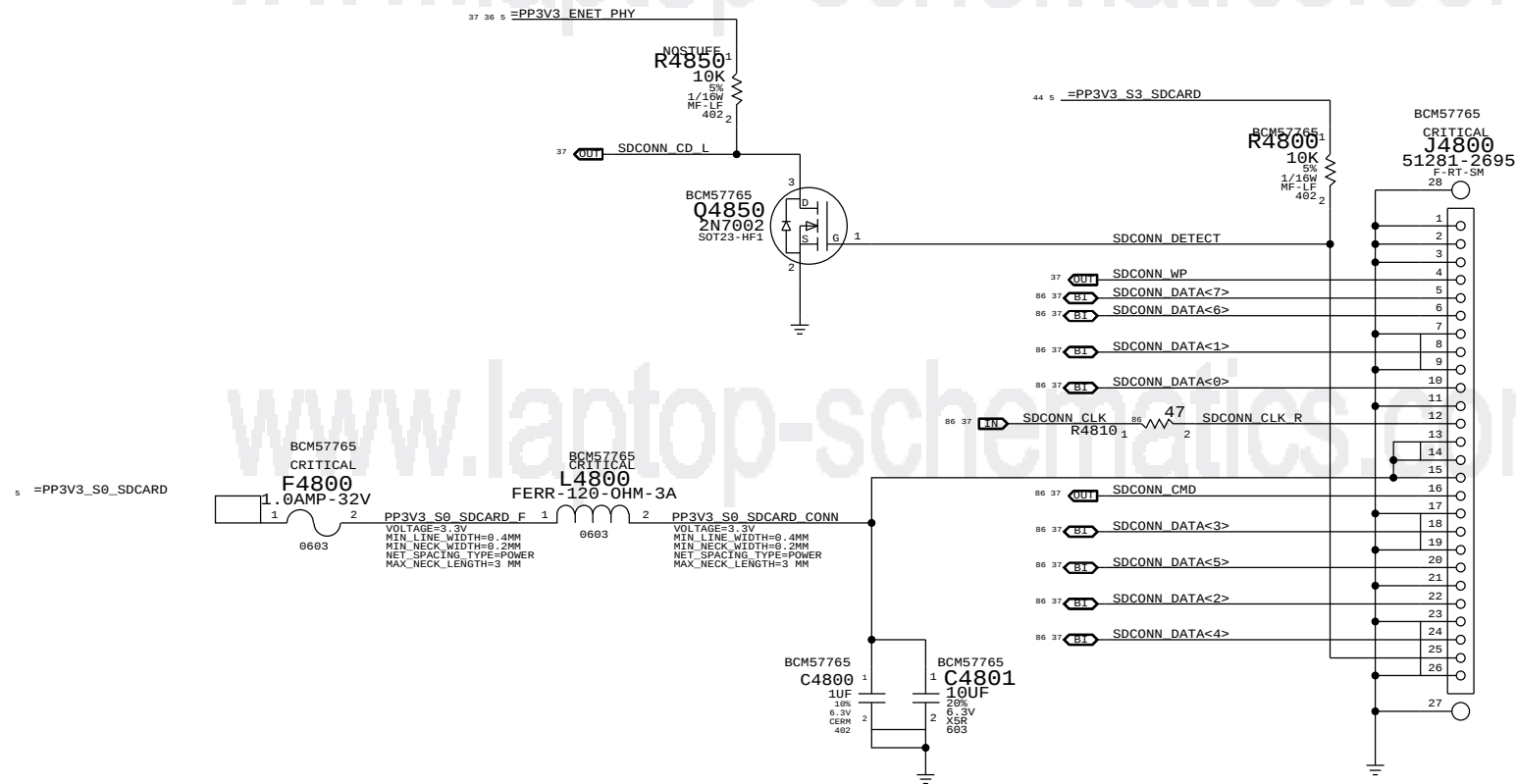


LAZAURS SD CARD READER BOARD CONNECTOR BACKUP TO CAESAR IV



SYNC MASTER=MASTER		SYNC DATE=11/06/2009	
PAGE TITLE		Internal USB Connections	
Apple Inc.		DRAWING NUMBER	051-8337
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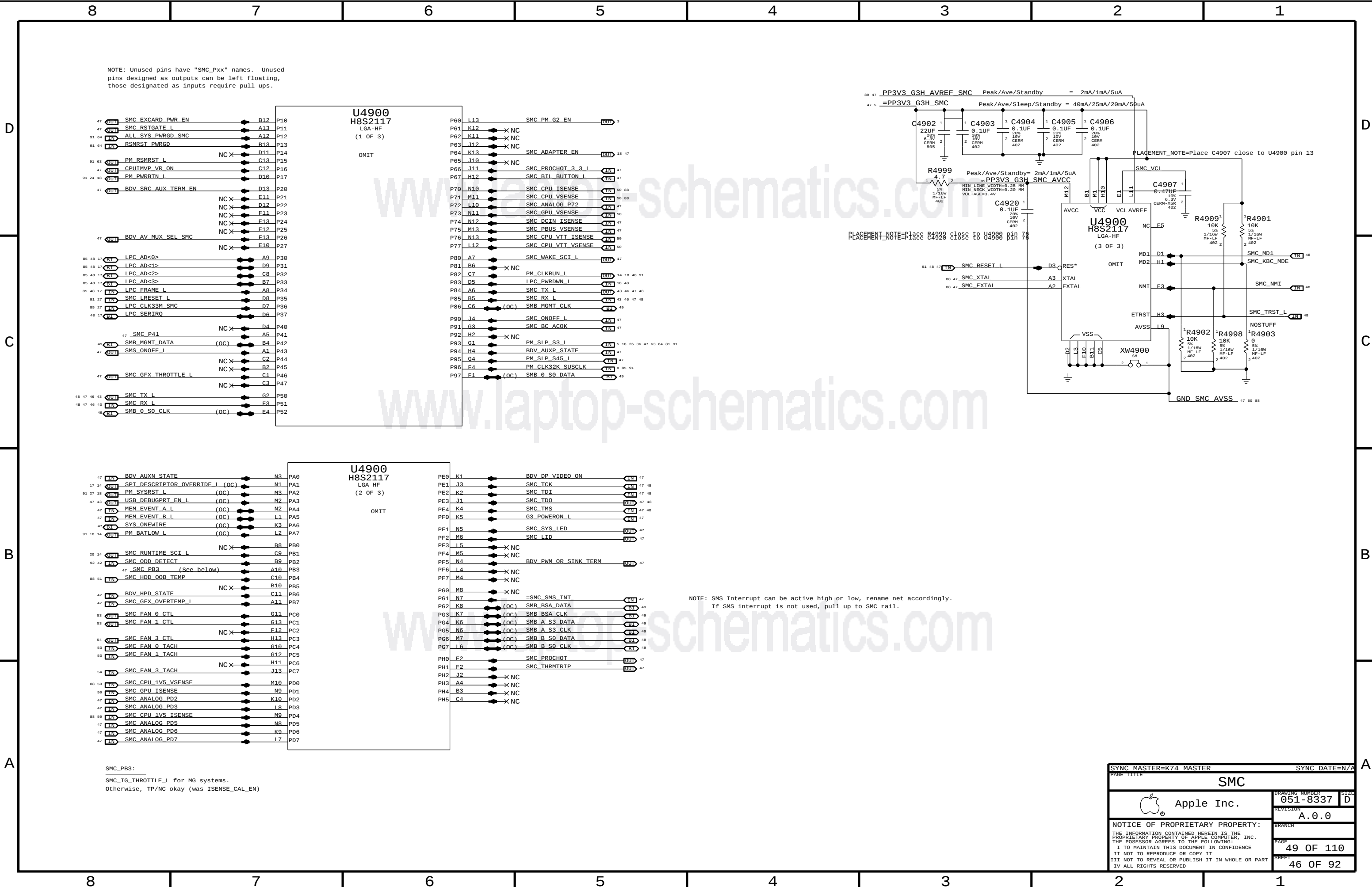
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IMAC CARD DETECT SWITCH IS NORMALLY-CLOSED TO GND
(CARD INSERTED = OPEN)
CAESAR-IV CARD DETECT IS PROGRAMMABLE, BUT A SILICON BUG
MAKES THE ACTIVE-HIGH CASE UNUSABLE.

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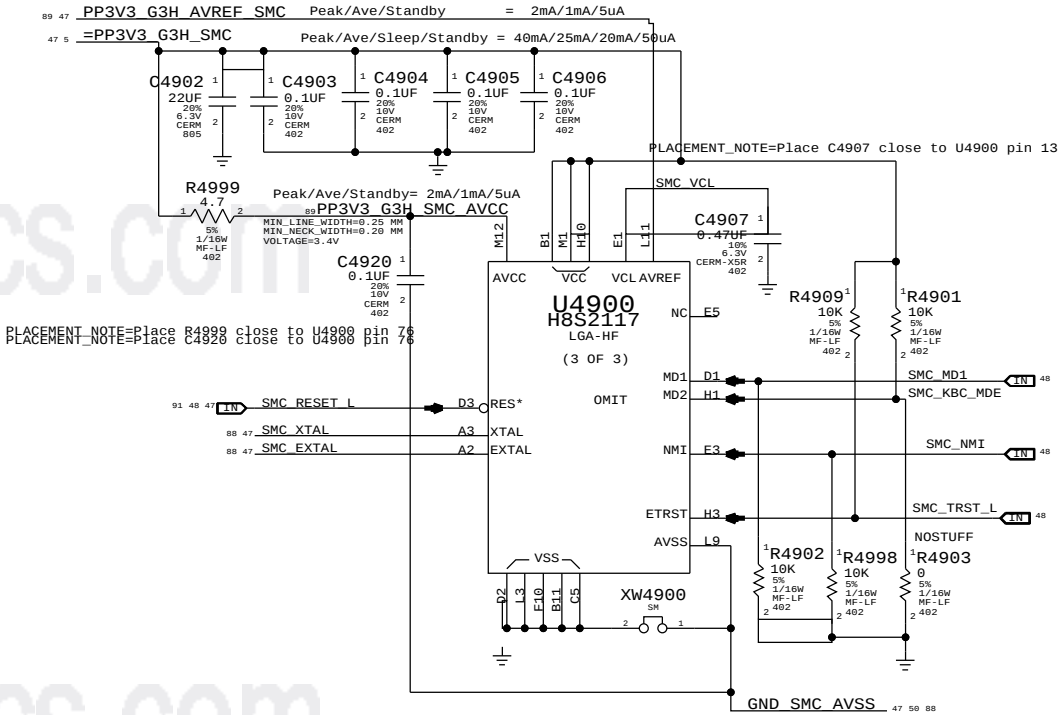
SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE		SD READER CONNECTOR	
 Apple Inc.		DRAWING NUMBER	051-8337
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		PAGE	48 OF 110
		SHEET	45 OF 92



NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

U4900
H8S2117
(1 OF 3)

OMIT



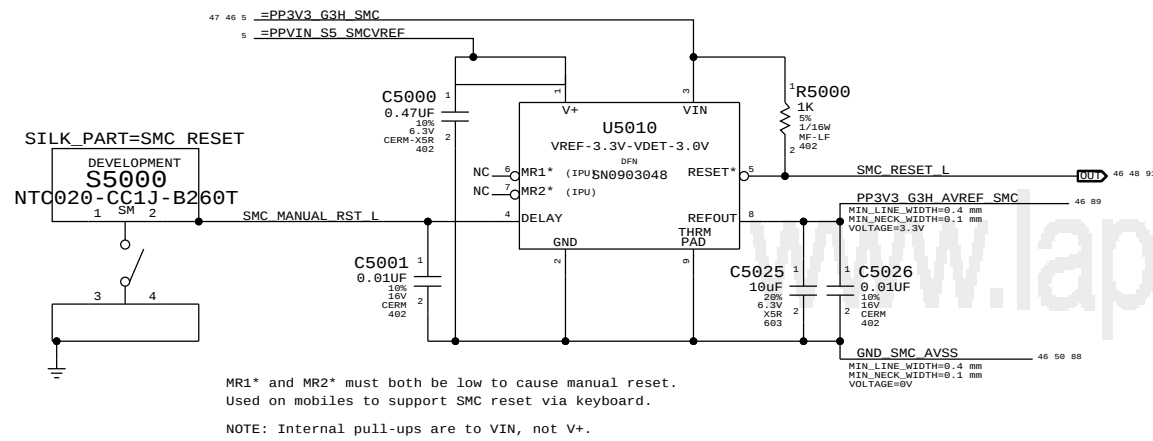
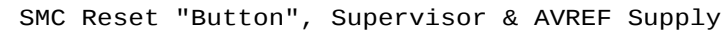
U4900
H8S2117
(2 OF 3)

OMIT

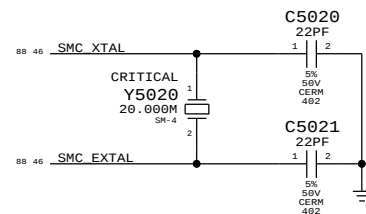
NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

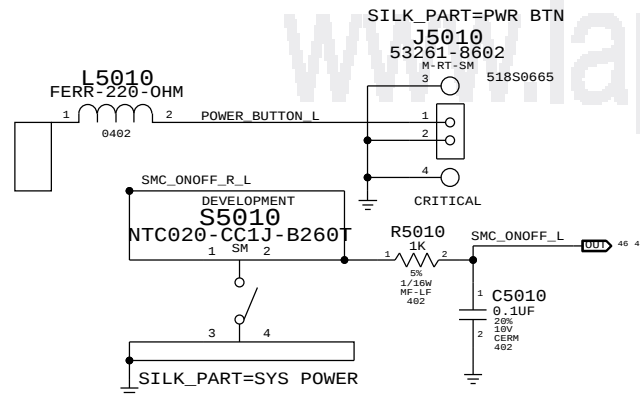
PAGE TITLE		PAGE TITLE	
SMC		SMC	
Apple Inc.		Apple Inc.	
DRAWING NUMBER		DRAWING NUMBER	
051-8337		051-8337	
REVISION		REVISION	
A.0.0		A.0.0	
BRANCH		BRANCH	
PAGE		PAGE	
49 OF 110		49 OF 110	
SHEET		SHEET	
46 OF 92		46 OF 92	



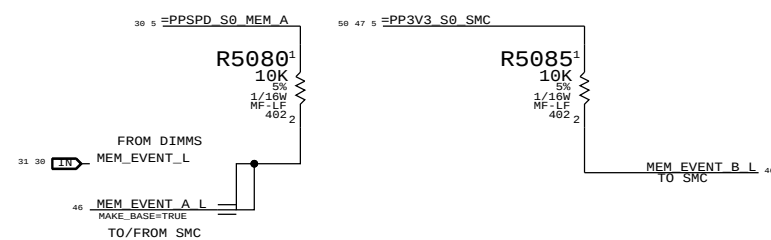
SMC Crystal Circuit



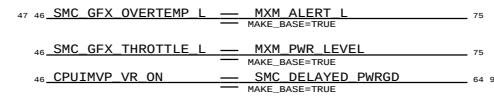
POWER BUTTON



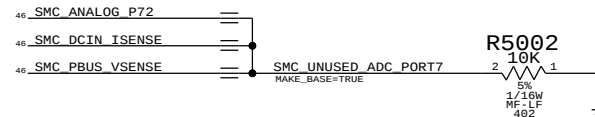
MEM_EVENT



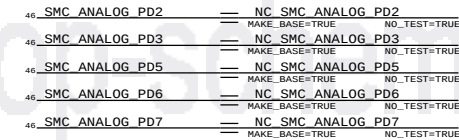
MISC. SIGNAL ALIASES



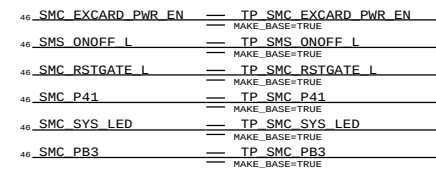
UNUSED PORT 7 ANALOG SENSORS



UNUSED PORT D ANALOG (INTERNAL PULLUPS)



UNUSED TP/NC ALIASES

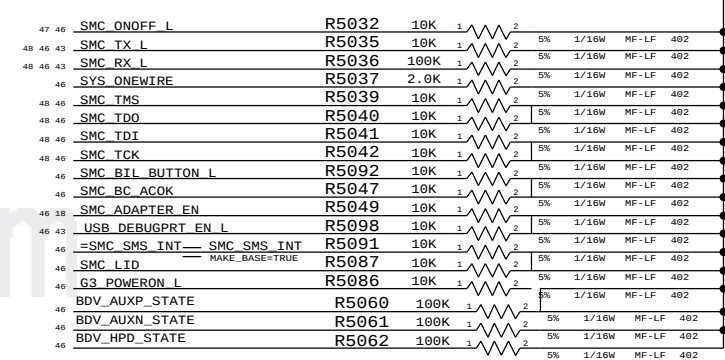


TIES OFF AUDIO DETECT CIRCUIT WHEN BIDIVI IS NOT USED

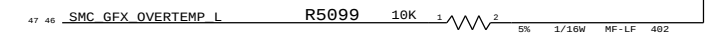
61 BDV_AV_MUX_SEL == GND AUDIO CODEC 56 57 61 62

MAKE_BASE=TRUE

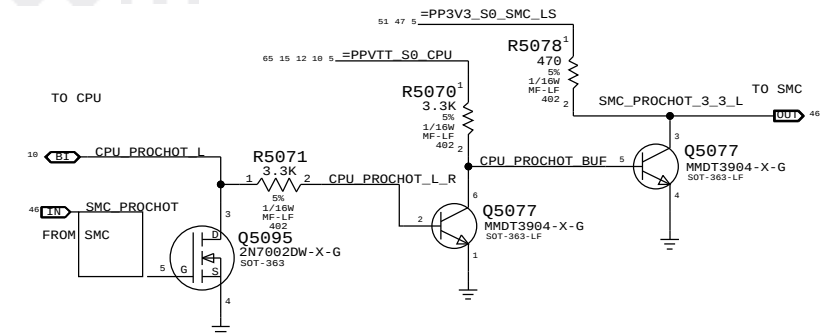
=PP3V3_G3H_SMC



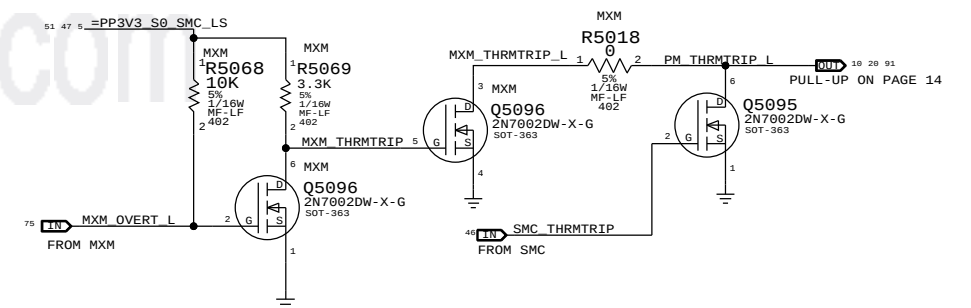
```
50 47 5 =PP3V3_S0_SMC
```



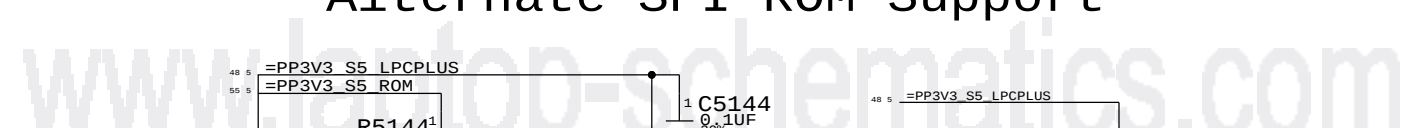
SMC PROCHOT 3.3V LEVEL SHIFTING

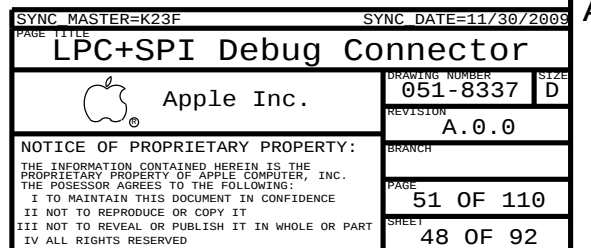


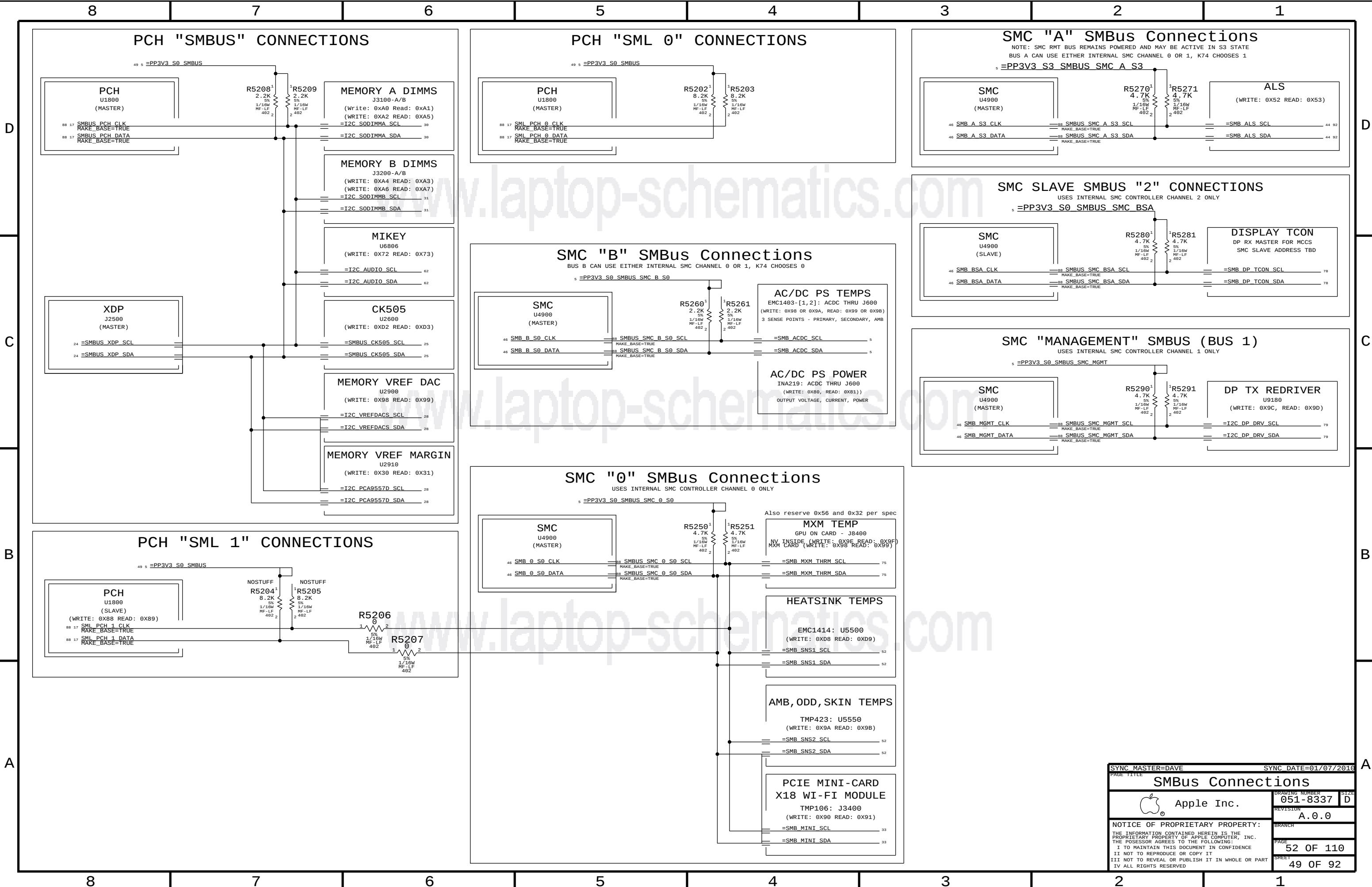
SMC & MXM THERMTRIP LEVEL SHIFTING



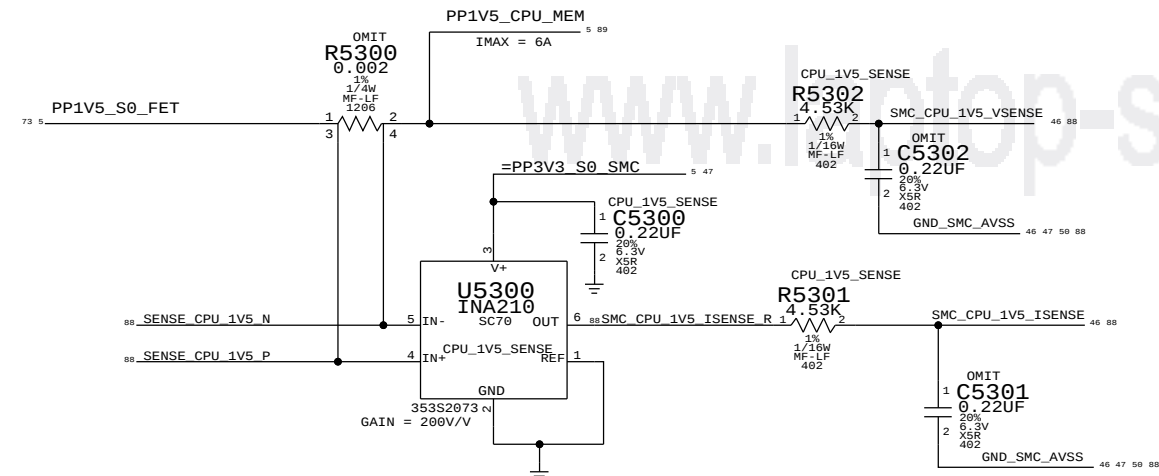
Pin	Signal	Pin	Signal
85 48	SPI ALT MOSI	10	SPIROM USE MLB
85 48	SPI ALT MISO	11	SPI ALT CLK
85 46 17	LPC FRAME L	13	SPI ALT CS L
91 46 18 14	PM CLKRUN L	14	LPC SERIO
47 46	SMC TMS	16	LPC PWRDWN L
91 27	DEBUG RESET L	17	SMC TDI





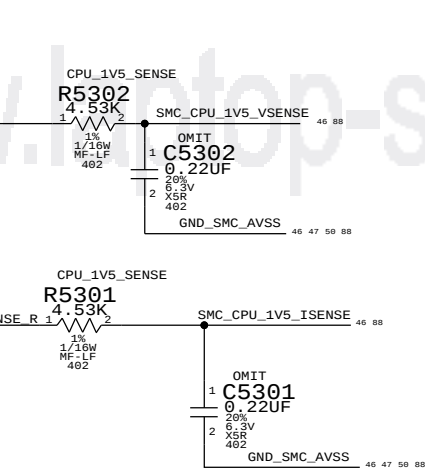


CPU 1.5V CURRENT SENSE

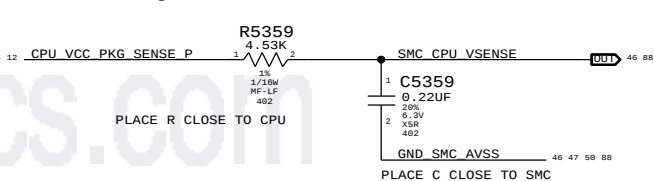


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES, 2 MILLIOHM, 1206	R5300	CPU_1V5_SENSE
101S0414	1	RES, 0 OHM, 1206, 20 MILLIOHM MAX	R5300	PRODUCTION
132S0080	2	CAP, 0.22UF, 402	C5301, C5302	CPU_1V5_SENSE
116S0004	2	RES, 0 OHM, 402	C5301, C5302	PRODUCTION

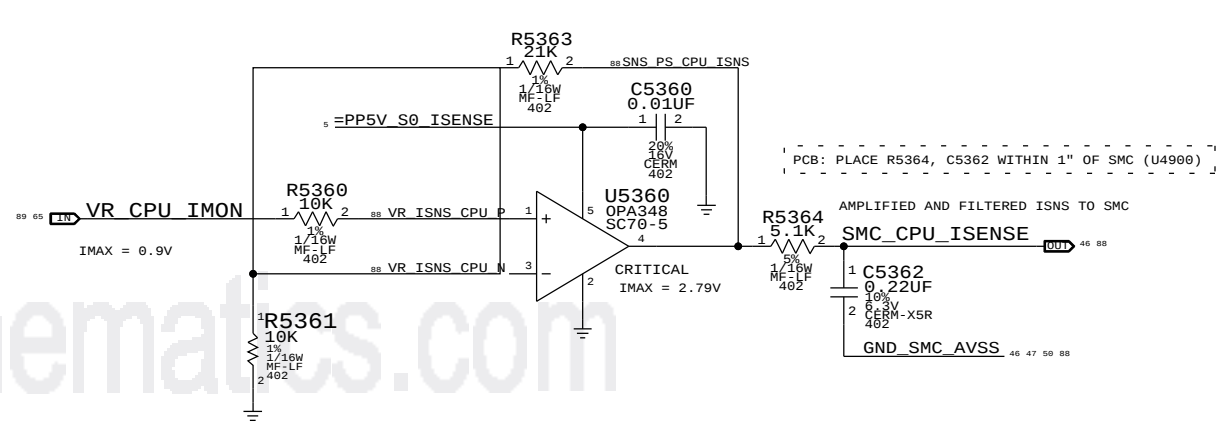
CPU 1.5V VOLTAGE SENSE



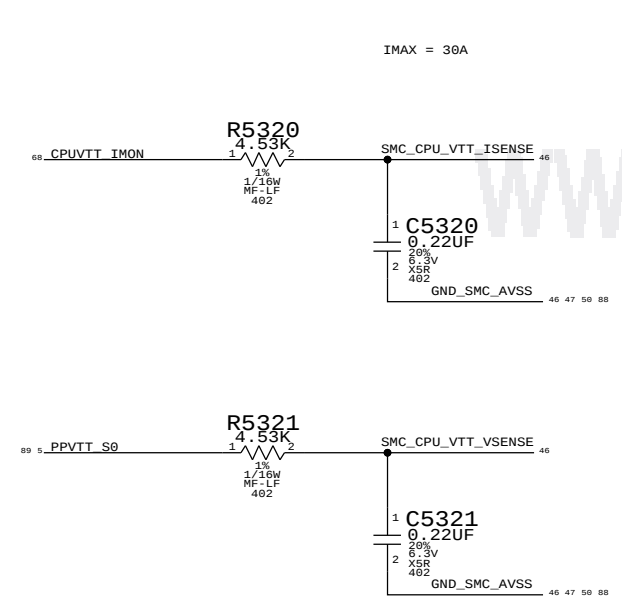
CPU Voltage Sense / Filter



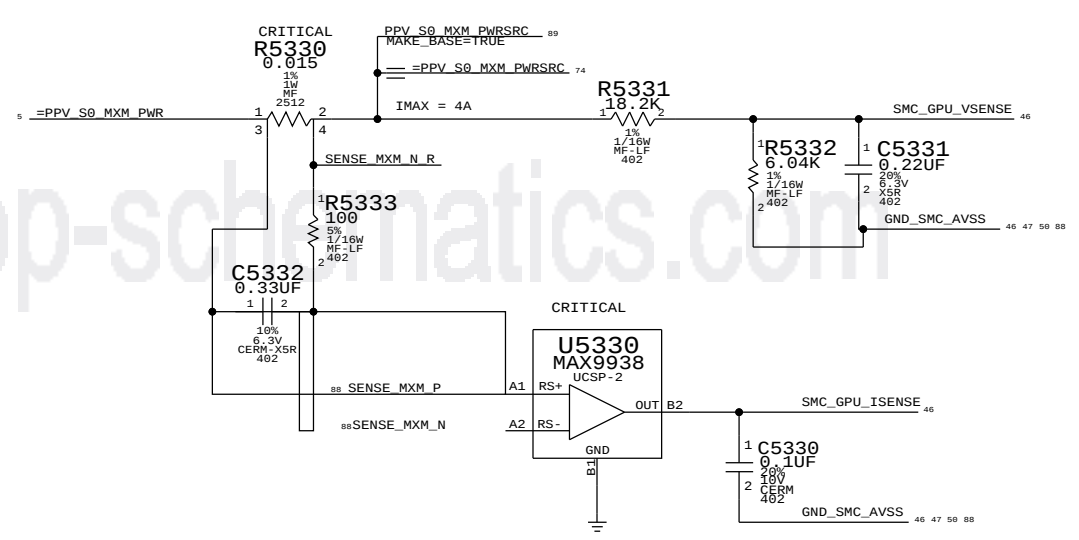
CPU CURRENT SENSE AMP & FILTER



CPU VTT CURRENT SENSE



MXM PWRSRC CURRENT & VOLTAGE SENSE



SYNC MASTER=K74 MASTER

SYNC DATE=N/A

CPU/GPU POWER SENSE

Apple Inc.

051-8337

A.0.0

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50 OF 92

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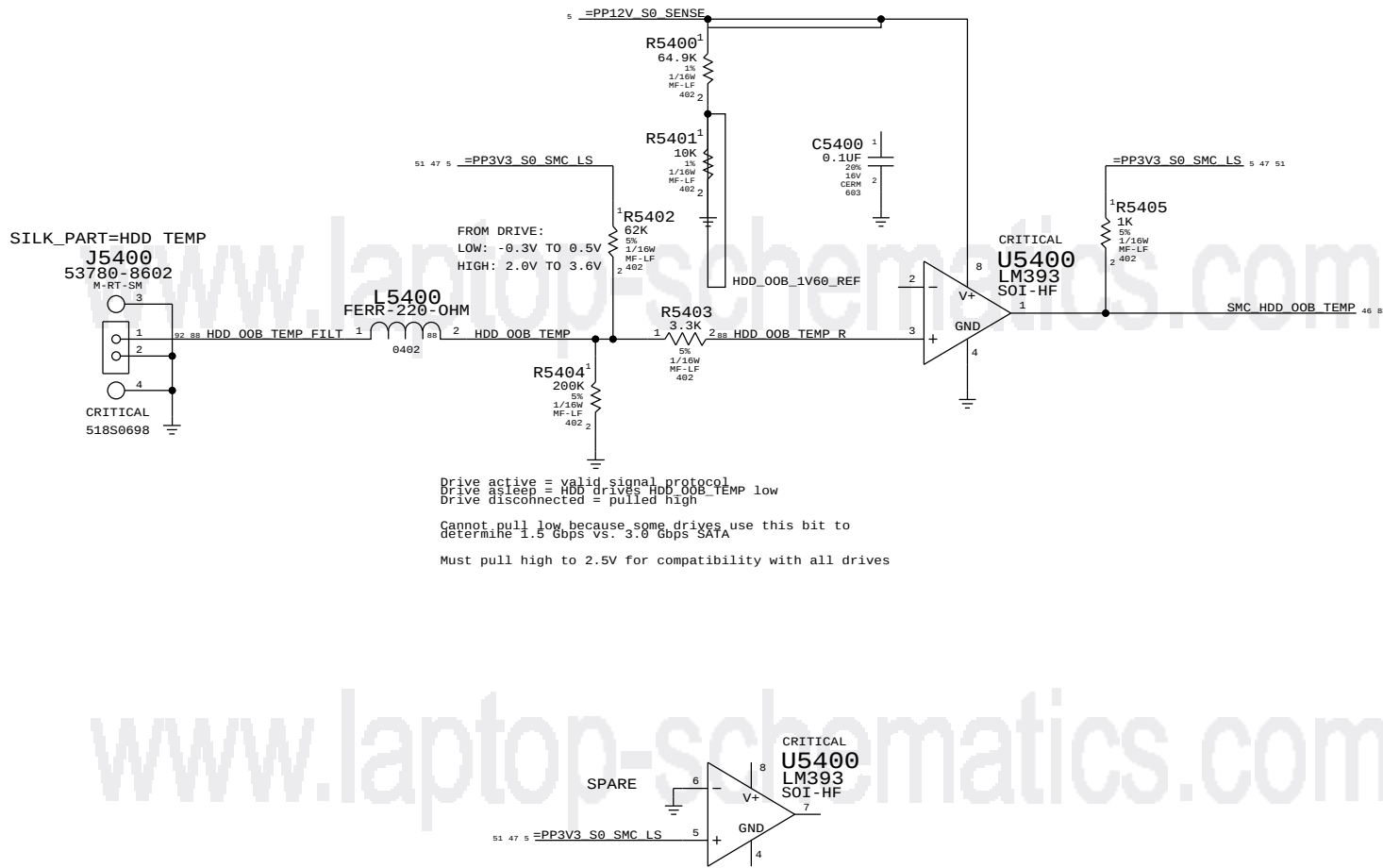
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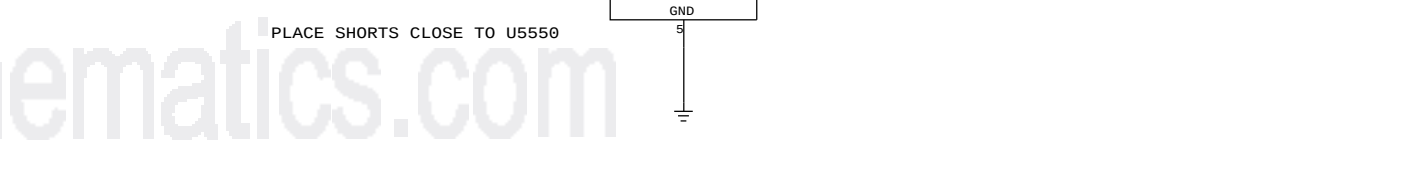
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HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



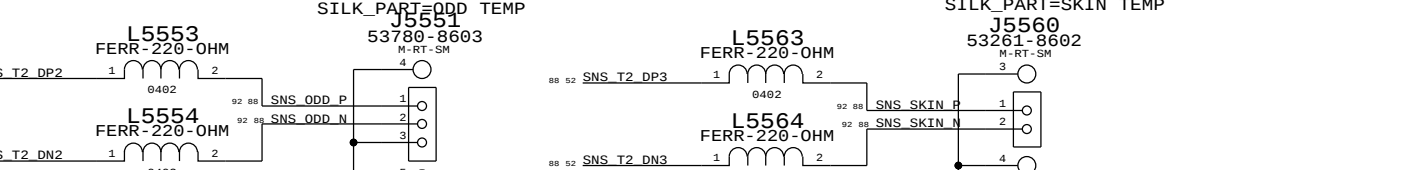
SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE		HDD TEMP SENSE	
DRAWING NUMBER		051-8337	SIZE D
REVISION		A.0.0	BRANCH
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The schematic diagram illustrates the sensor module's internal components and their connections. It is divided into two main sections based on the `SILK_PART` configuration:

- SILK_PART=MXM OR CPU:** This section shows a sensor module with a 4-pin connector (pins 1, 2, 3, 4) connected to the CPU/Sensor module. The module includes a 53398-8602 (M-ST-SH) component, a 53780-8603 (M-RT-SH) component, and a 53780-8603 (M-RT-SH) component. It also features a 53780-8603 (M-RT-SH) component and a 53780-8603 (M-RT-SH) component.
- SILK_PART=MXM HSK:** This section shows a sensor module with a 4-pin connector (pins 1, 2, 3, 4) connected to the CPU/Sensor module. The module includes a 53398-8602 (M-ST-SH) component, a 53780-8603 (M-RT-SH) component, and a 53780-8603 (M-RT-SH) component. It also features a 53780-8603 (M-RT-SH) component and a 53780-8603 (M-RT-SH) component.

The diagram also shows the connection to the CPU/Sensor module via a 4-pin connector (pins 1, 2, 3, 4). The module includes a 53398-8602 (M-ST-SH) component, a 53780-8603 (M-RT-SH) component, and a 53780-8603 (M-RT-SH) component. It also features a 53780-8603 (M-RT-SH) component and a 53780-8603 (M-RT-SH) component.



BIASENT SENSE CONNECTOR COMBINED WITH CPU FAN

L5522
FERR-220-0HM

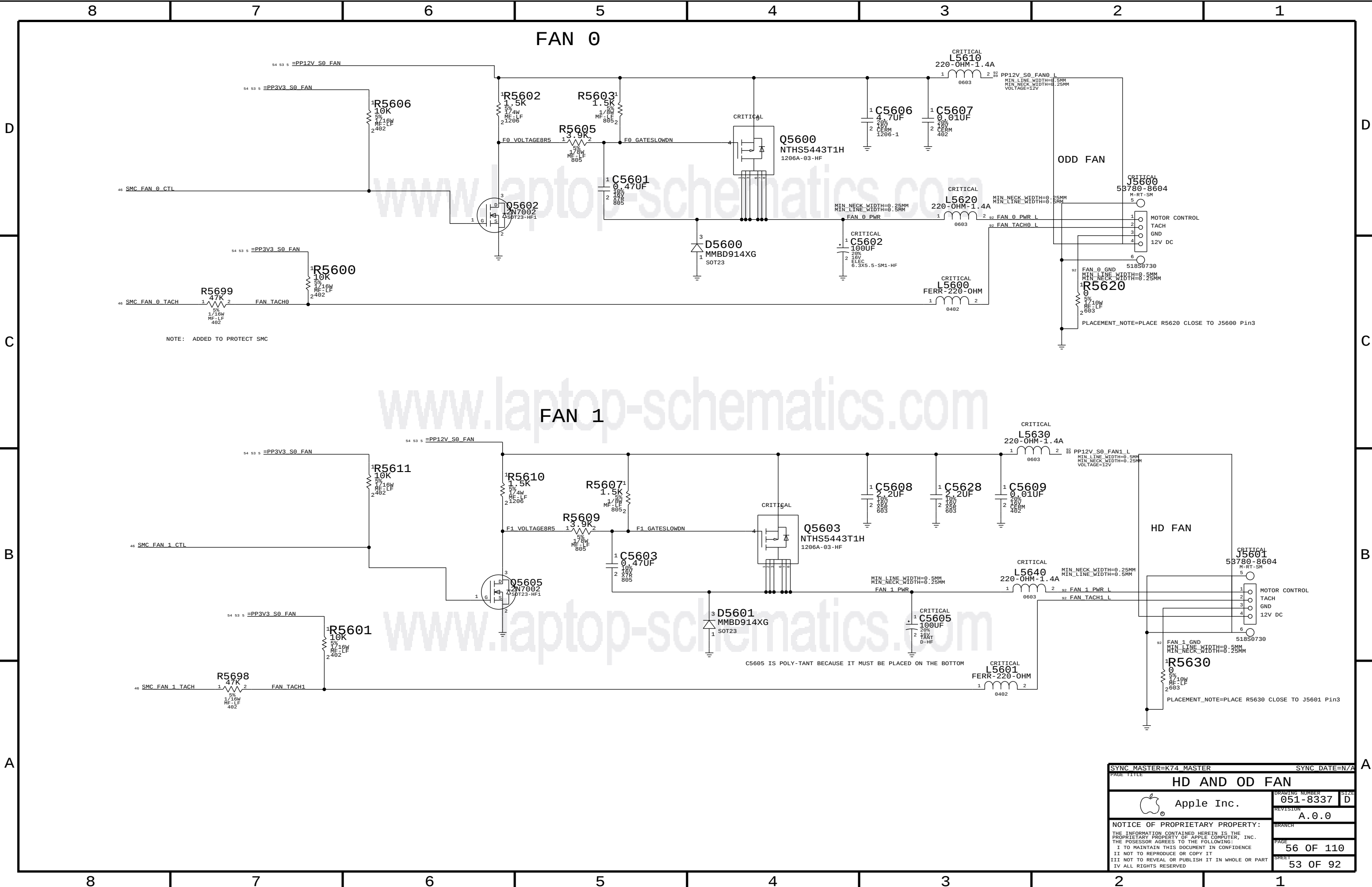
SNS_T2_DP1 1 2

0402

L5523
FERR-220-0HM

SNS_AMB_P 54 88 92
SNS_AMB_N 54 88 92

SYNC MASTER=NICK		SYNC DATE=11/06/2005	
PAGE 1 OF 1			
REMOTE TEMP/POWER SENSORS			
	Apple Inc.		DRAWING NUMBER
			051-8337
			SIZE
			D
		REVISION	
		A.0.0	
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		PAGE	
		55 OF 110	
		SHEET	
		52 OF 92	

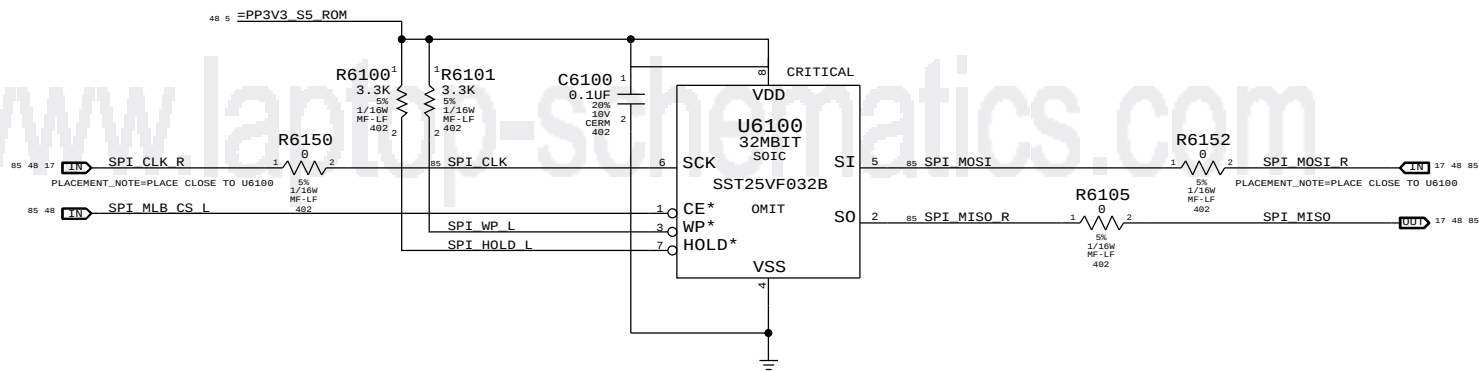


SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE			
HD AND OD FAN			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-8337		D
	REVISION		A.0.0
BRANCH			
PAGE			
56 OF 110			
SHEET			
53 OF 92			



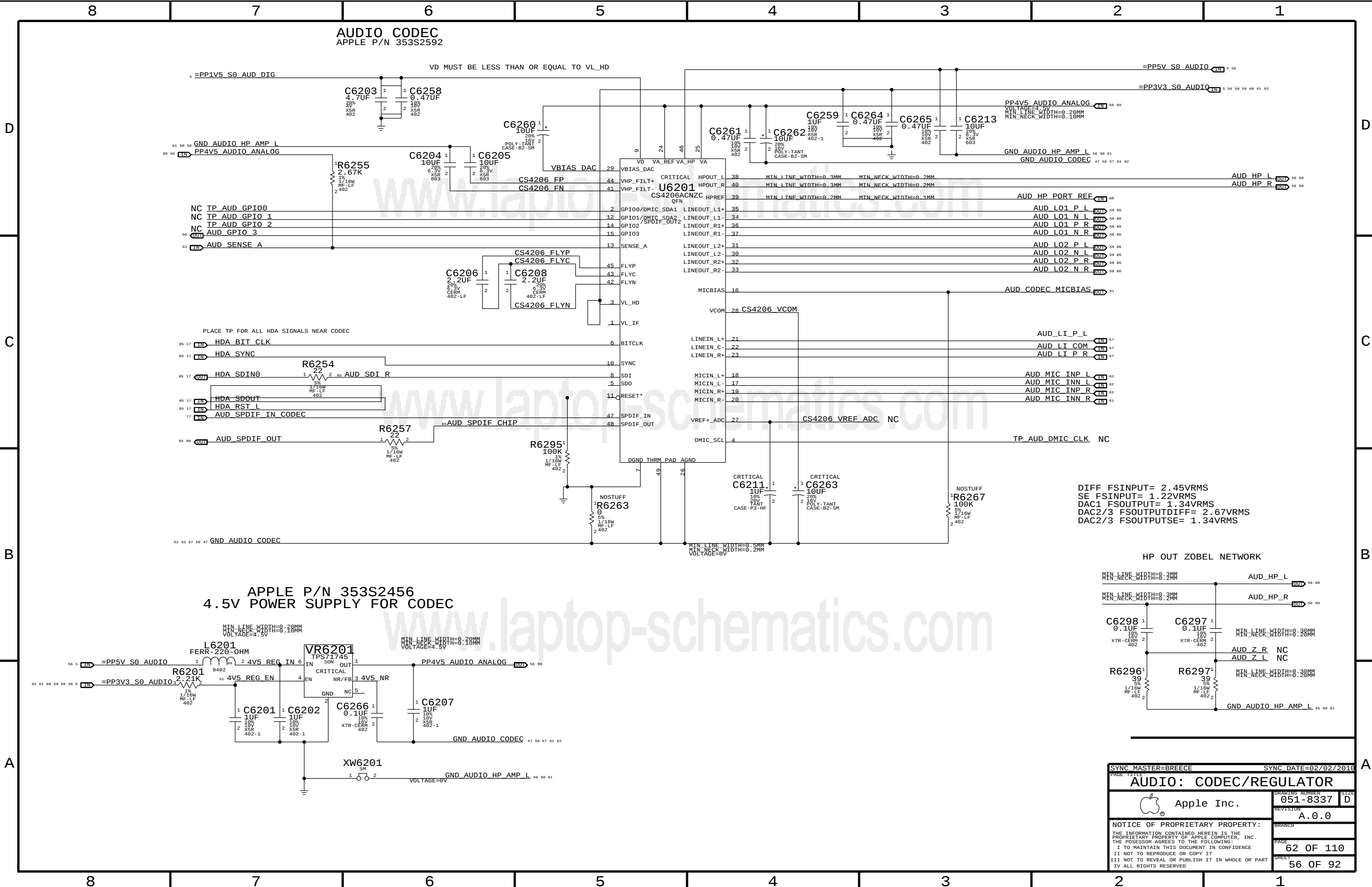
PAGE TITLE		DRAWING NUMBER		SIZE	
CPU FAN & AMBIENT SENSE		051-8337		D	
 Apple Inc.		REVISION		A.0.0	
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		SHEET		54 OF 92	

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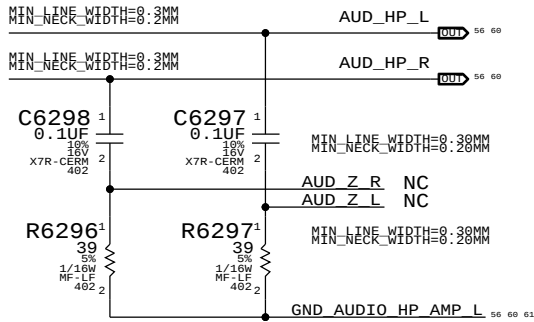
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SYNC MASTER=K23F		SYNC DATE=11/30/2009	
PAGE TITLE		SPI ROM	
DRAWING NUMBER		051-8337	D
REVISION		A.0.0	
BRANCH			
PAGE		61 OF 110	
SHEET		55 OF 92	
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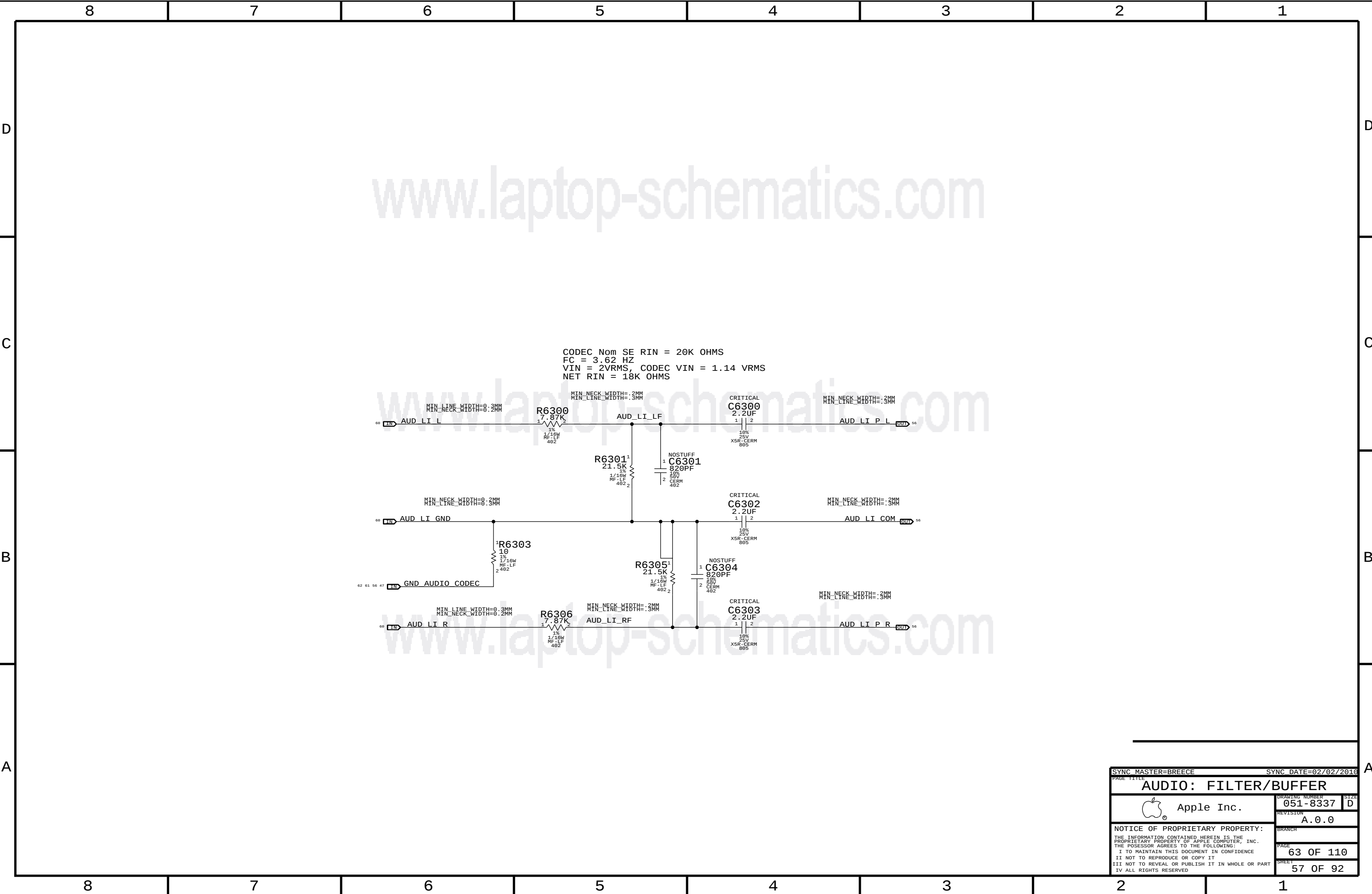


DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

HP OUT ZOBEL NETWORK

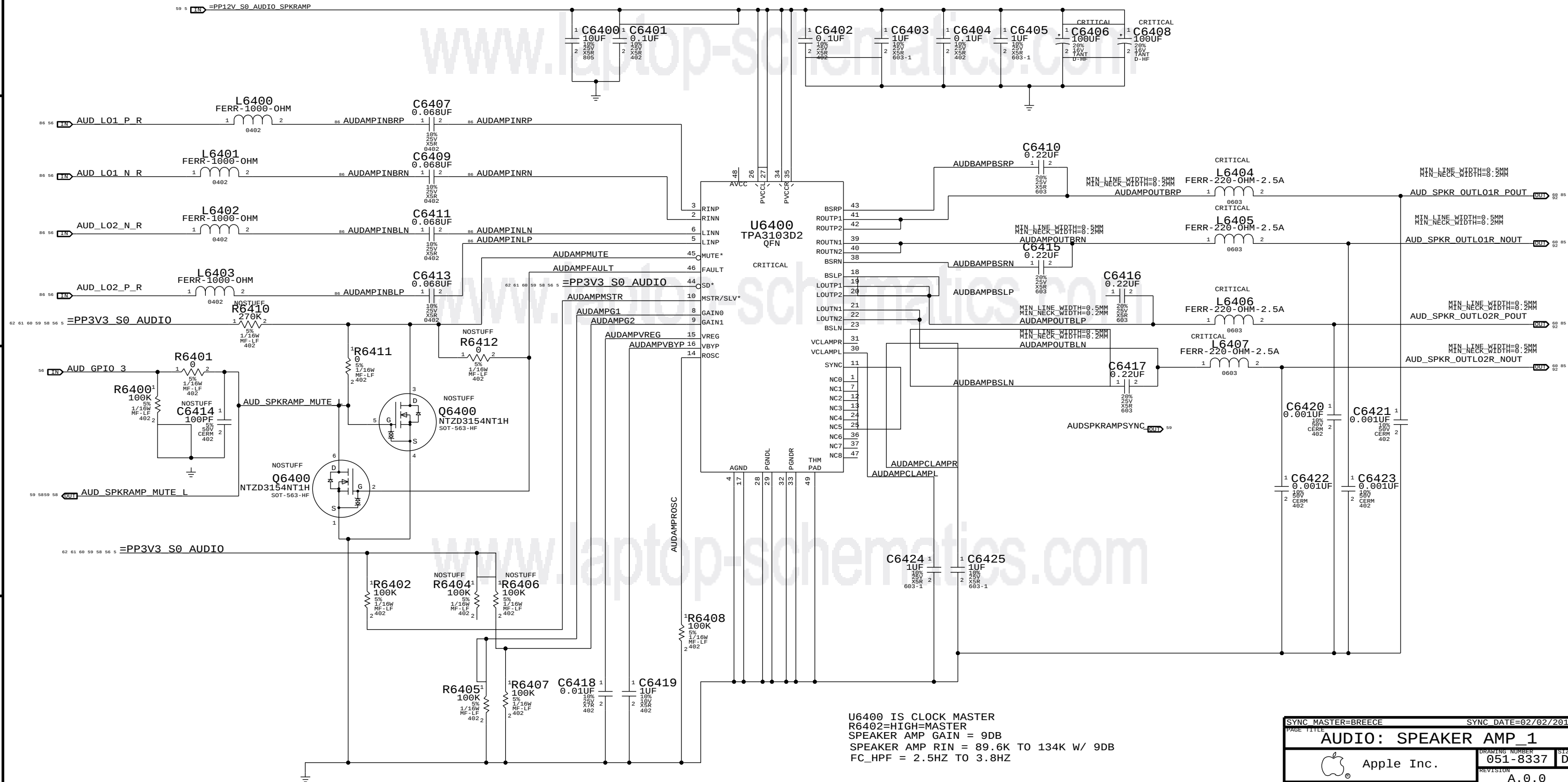


SYNC MASTER=BREECE		SYNC DATE=02/02/2016	
PAGE TITLE		AUDIO: CODEC/REGULATOR	
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SYNC MASTER=BREECE		SYNC DATE=02/02/2016	
PAGE TITLE			
AUDIO: FILTER/BUFFER			
Apple Inc.		DRAWING NUMBER	051-8337
		REVISION	A.0.0
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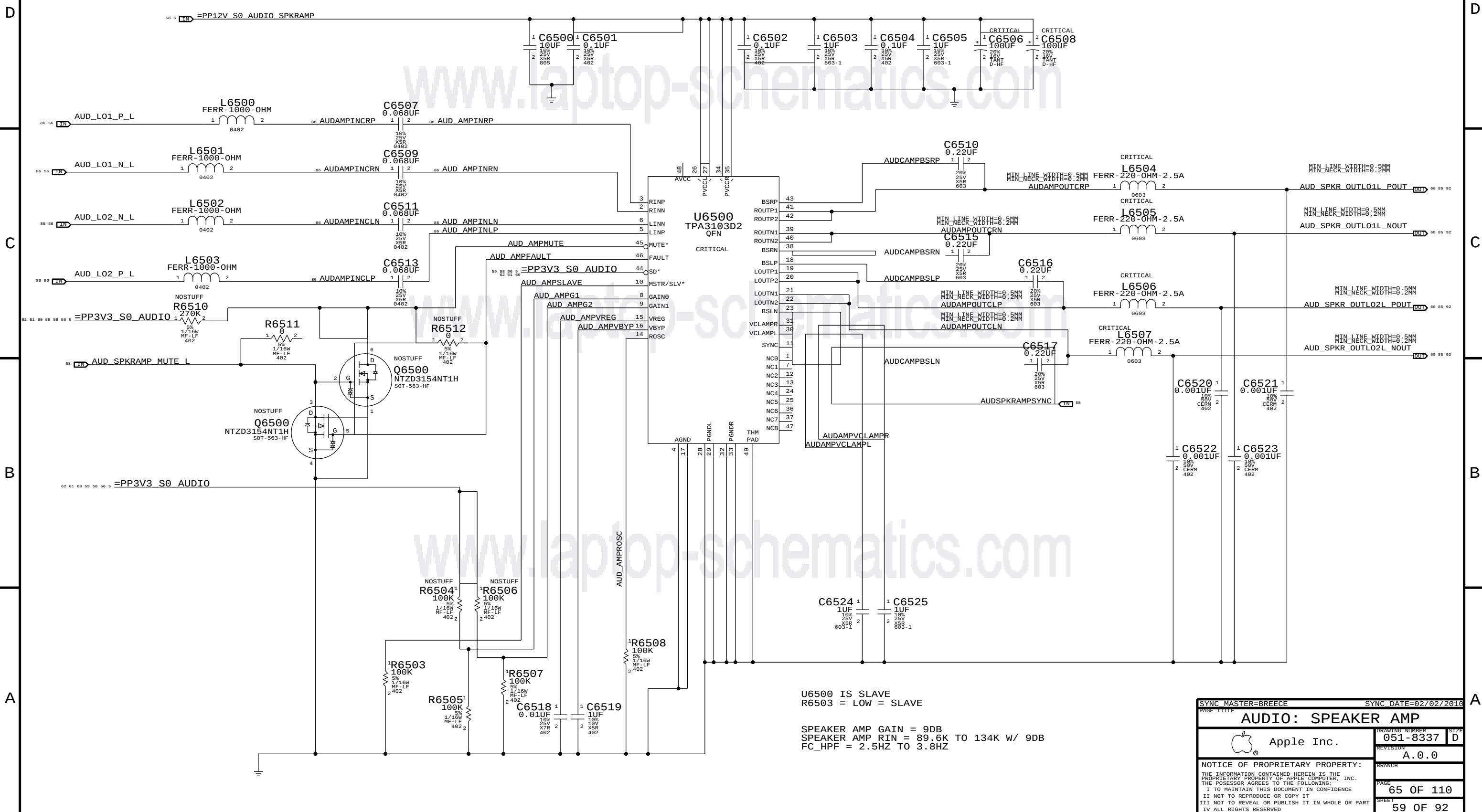
RIGHT CH. SPEAKER AMP
APPLE P/N 353S2768



U6400 IS CLOCK MASTER
R6402=HIGH=MASTER
SPEAKER AMP GAIN = 9DB
SPEAKER AMP RIN = 89.6K TO 134K W/ 9DB
FC_HPF = 2.5HZ TO 3.8HZ

PAGE TITLE		PAGE TITLE	
AUDIO: SPEAKER AMP_1		051-8337	
Apple Inc.		A.0.0	
NOTICE OF PROPRIETARY PROPERTY:		64 OF 110	
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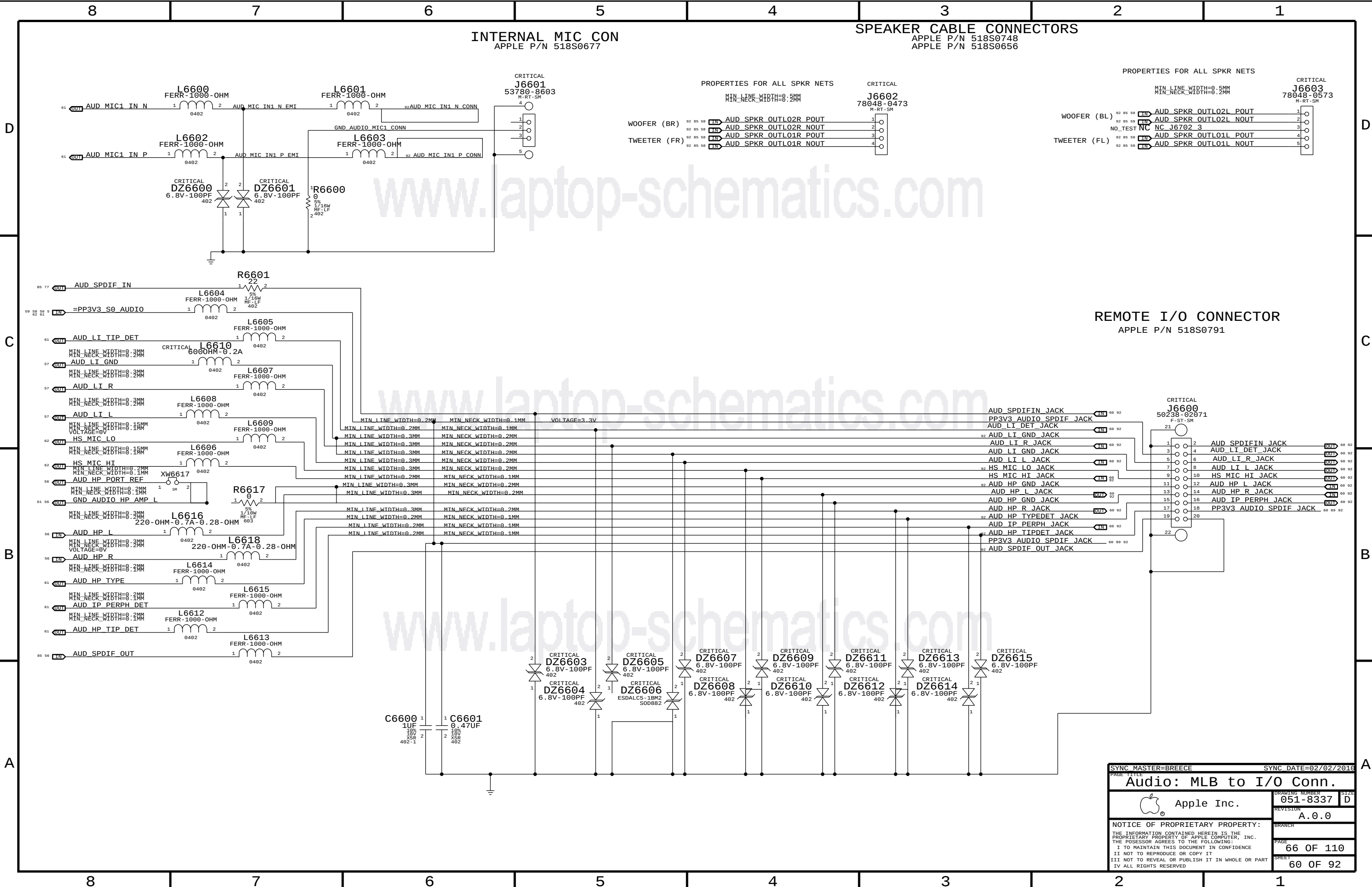
LEFT CH. SPEAKER AMP
APPLE P/N 353S2768



U6500 IS SLAVE
R6503 = LOW = SLAVE

SPEAKER AMP GAIN = 9DB
SPEAKER AMP RIN = 89.6K TO 134K W/ 9DB
FC_HPFB = 2.5HZ TO 3.8HZ

PAGE TITLE		SYNC DATE=02/02/2016	
AUDIO: SPEAKER AMP		DRAWING NUMBER	
Apple Inc.		051-8337	
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		59 OF 92	



INTERNAL MIC CON
APPLE P/N 518S0677

SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656

PROPERTIES FOR ALL SPKR NETS

MIN LINE WIDTH=0.5MM
MIN NECK WIDTH=0.2MM

CRITICAL
J6603
53780-8603
M-RT-SM

PROPERTIES FOR ALL SPKR NETS

MIN LINE WIDTH=0.5MM
MIN NECK WIDTH=0.2MM

CRITICAL
J6602
78048-0473
M-RT-SM

WOOFER (BR)	AUD SPKR OUTL02R POUT	AUD SPKR OUTL02R NOUT
92 85 58	1	2
92 85 58	3	4

TWEETER (FR)	AUD SPKR OUTL01R POUT	AUD SPKR OUTL01R NOUT
92 85 58	1	2
92 85 58	3	4

PROPERTIES FOR ALL SPKR NETS

MIN LINE WIDTH=0.5MM
MIN NECK WIDTH=0.2MM

CRITICAL
J6603
78048-0573
M-RT-SM

WOOFER (BL)	AUD SPKR OUTL02L POUT	AUD SPKR OUTL02L NOUT
92 85 58	1	2
92 85 58	3	4

TWEETER (FL)	AUD SPKR OUTL01L POUT	AUD SPKR OUTL01L NOUT
92 85 58	1	2
92 85 58	3	4

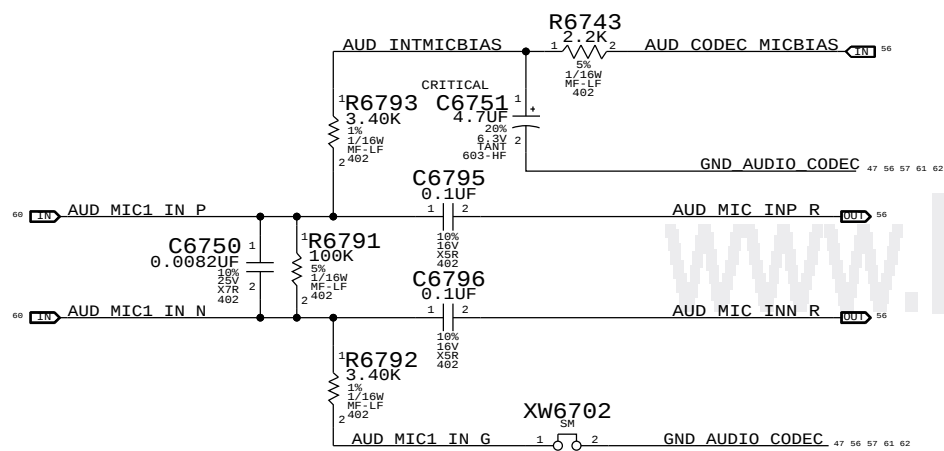
REMOTE I/O CONNECTOR
APPLE P/N 518S0791

CRITICAL
J6600
50238-02071
F-ST-SM

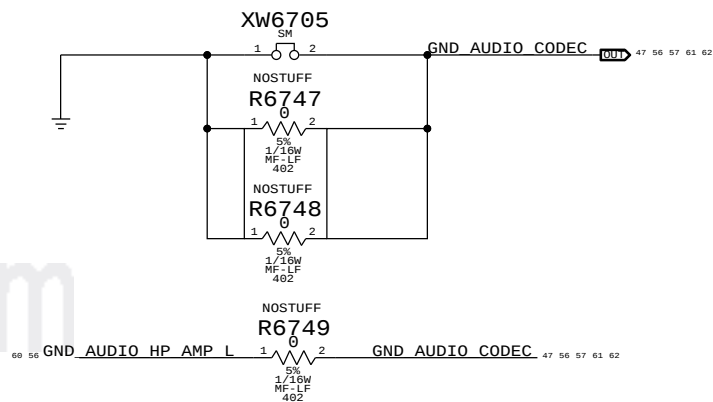
AUD SPDIFIN JACK	AUD LI DET JACK	AUD LI R JACK	AUD LI L JACK	HS MIC LO JACK	HS MIC HI JACK	AUD HP GND JACK	AUD HP L JACK	AUD HP R JACK	AUD HP GND JACK	AUD HP TYPEDET JACK	AUD IP PERPH JACK	PP3V3 AUDIO SPDIF JACK	AUD SPDIF OUT JACK
60 92	60 92	60 92	60 92	60 92	60 92	60 92	60 92	60 92	60 92	60 92	60 92	60 92	60 92

SYNC MASTER=BREECE		SYNC DATE=02/02/2016	
Audio: MLB to I/O Conn.			
Apple Inc.		DRAWING NUMBER	051-8337
		REVISION	A.0.0
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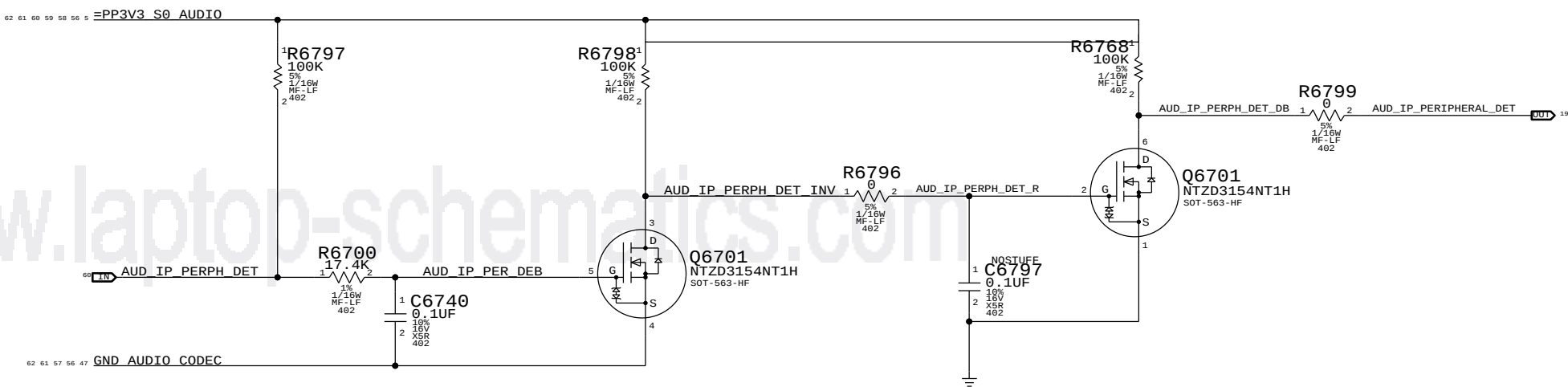
Internal Microphone Impedance Matching



AUDIO STAR GND AND STUFFING OPTIONS



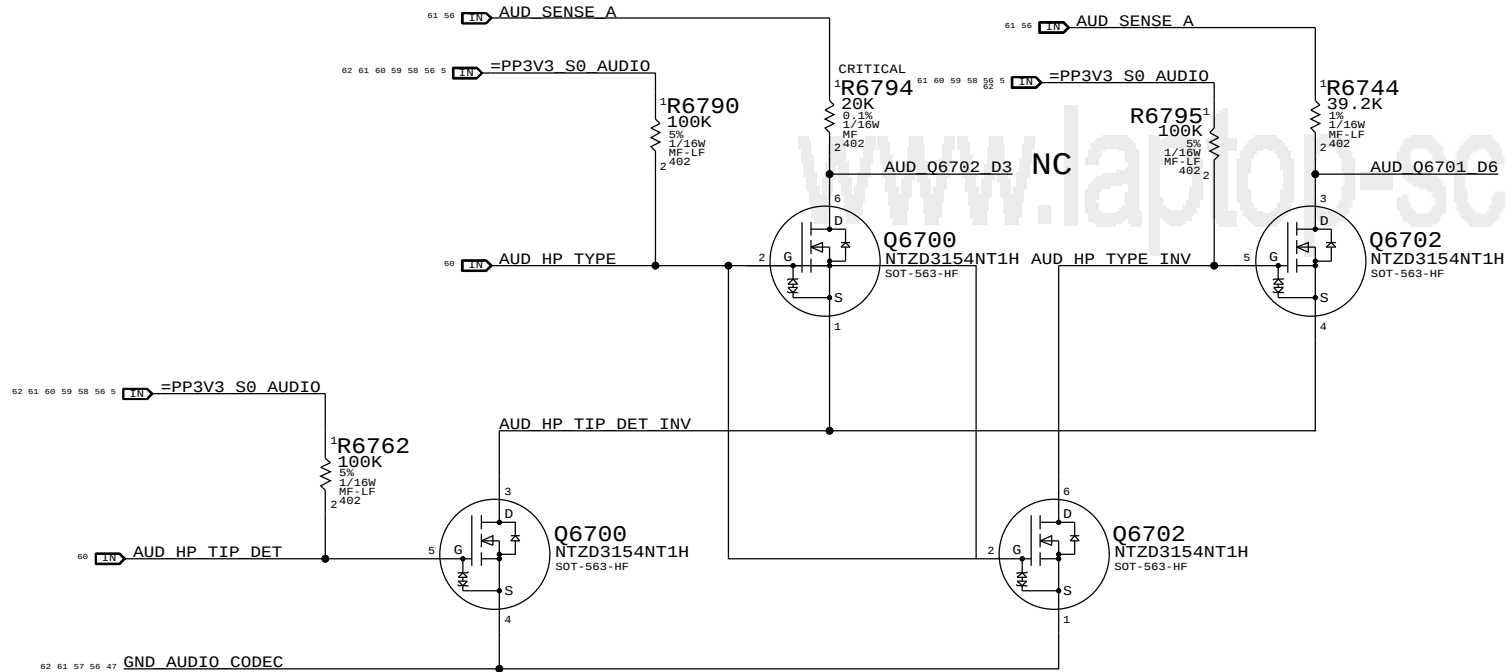
IPHS HS Detect Debounce CKT



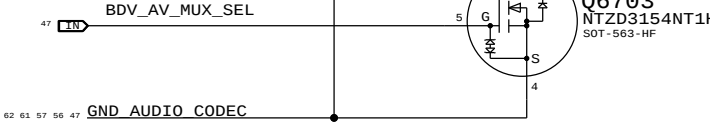
Digital Out

Headphone Out

LI Insert Detect



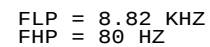
DP Audio Enable

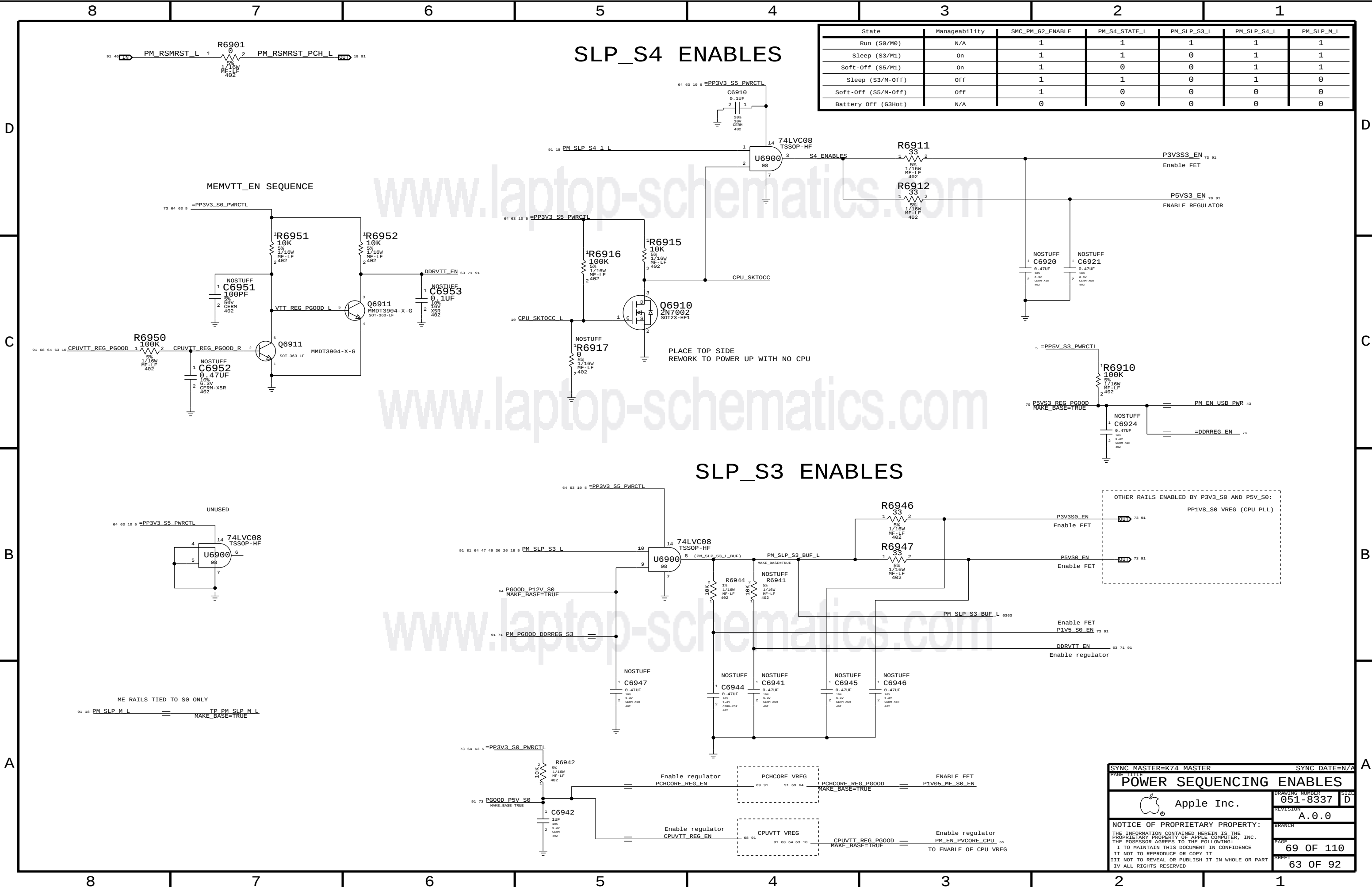


SYNC MASTER=BREECE		SYNC DATE=02/02/2016	
PAGE TITLE		AUDIO: Detects/Grounding	
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N/A N/A MCP GPIO_38 MCP GPIO_5

WRITE: 0X72 READ: 0X73 APN 353S2256





SLP_S4 ENABLES

State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SLP_S3 ENABLES

SYNC MASTER=K74 MASTER

SYNC DATE=N/A

POWER SEQUENCING ENABLES

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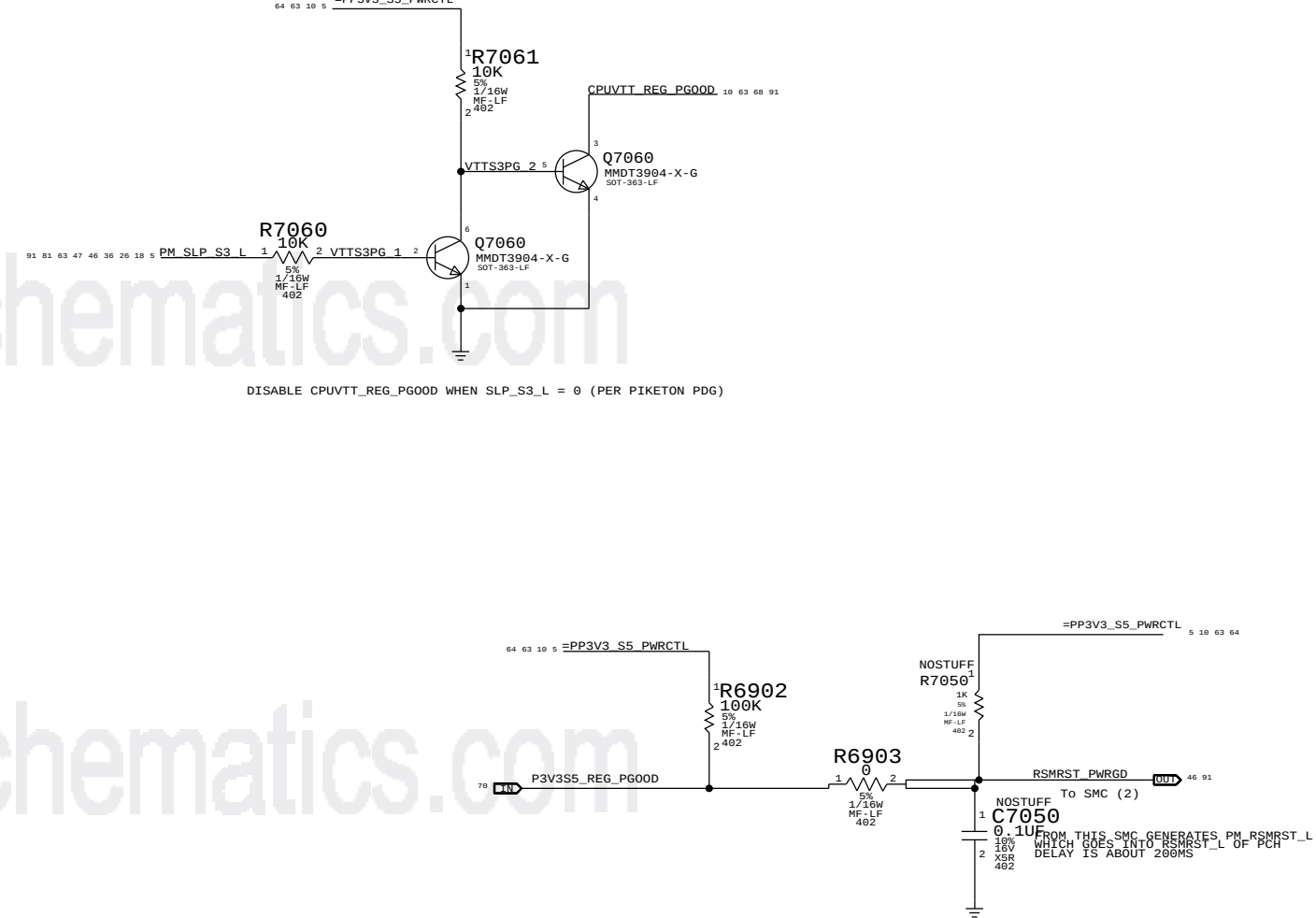
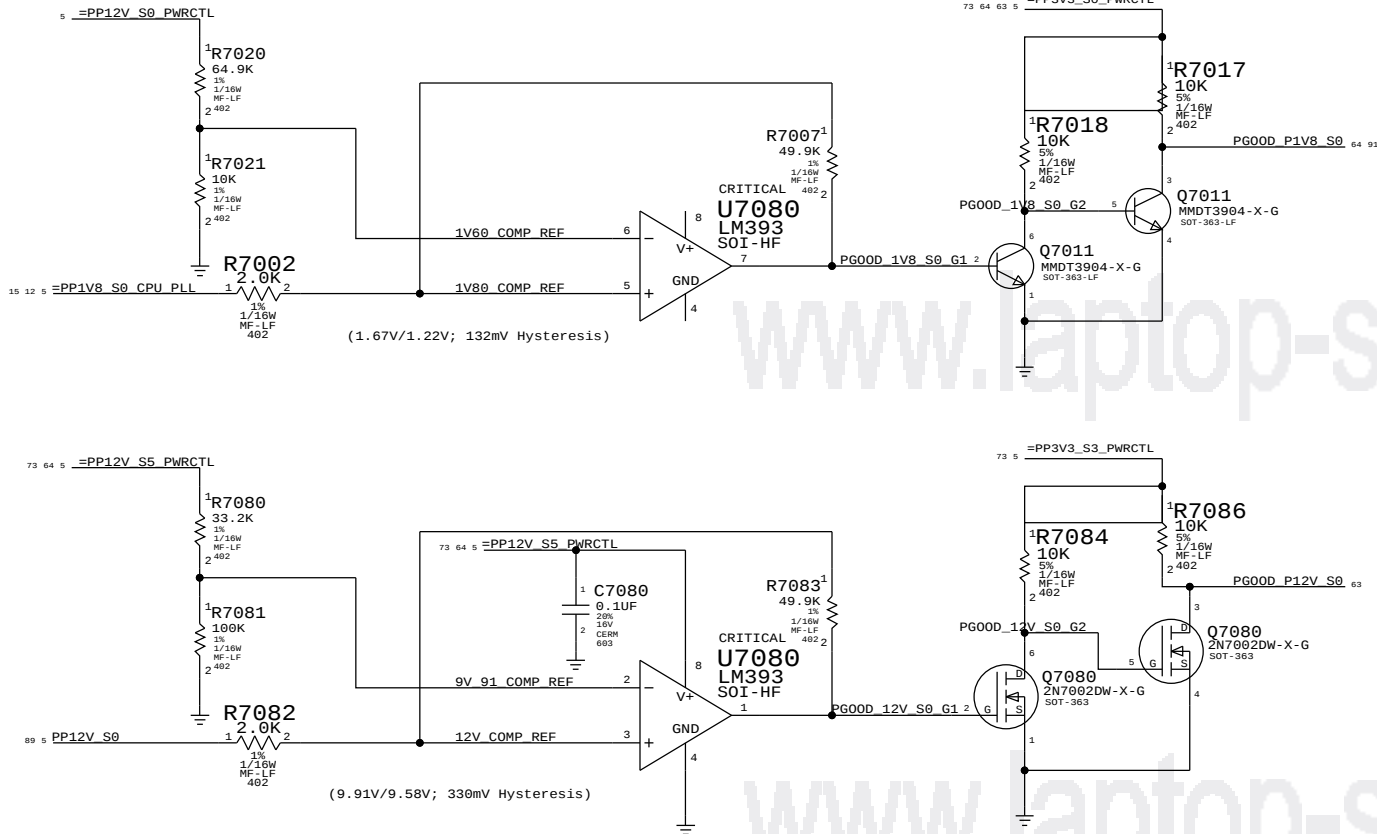
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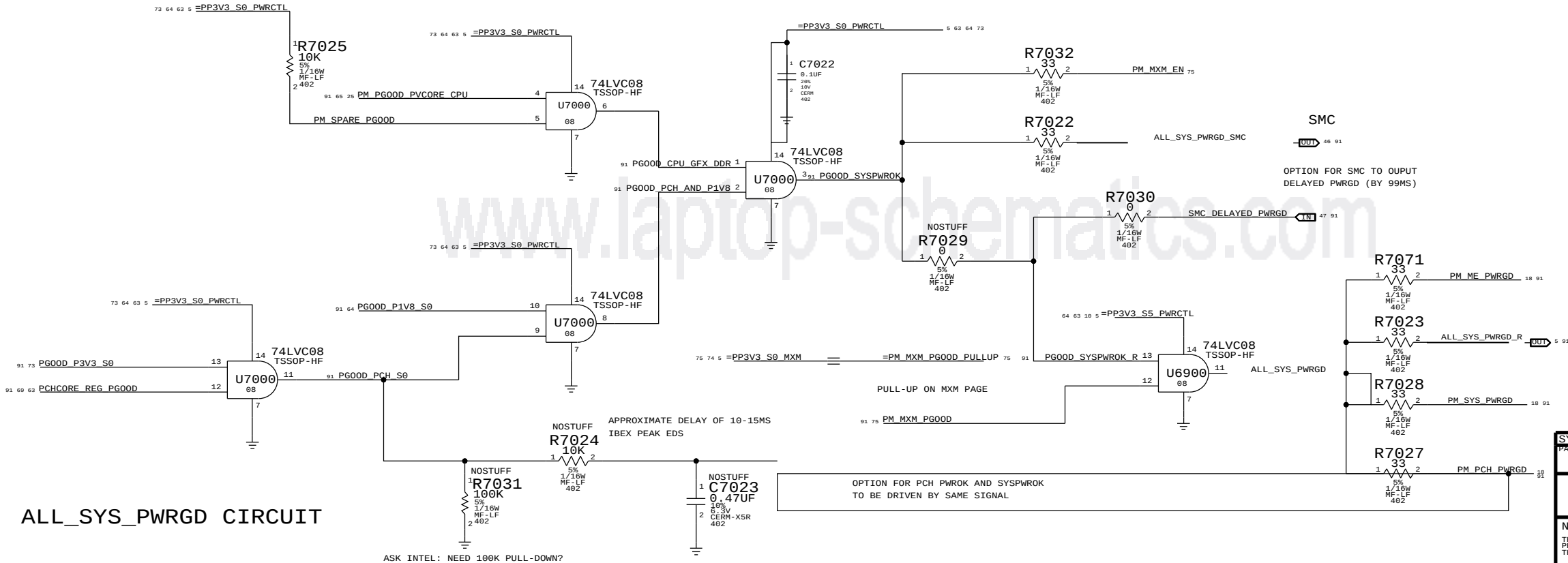
69 OF 110

63 OF 92

PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0

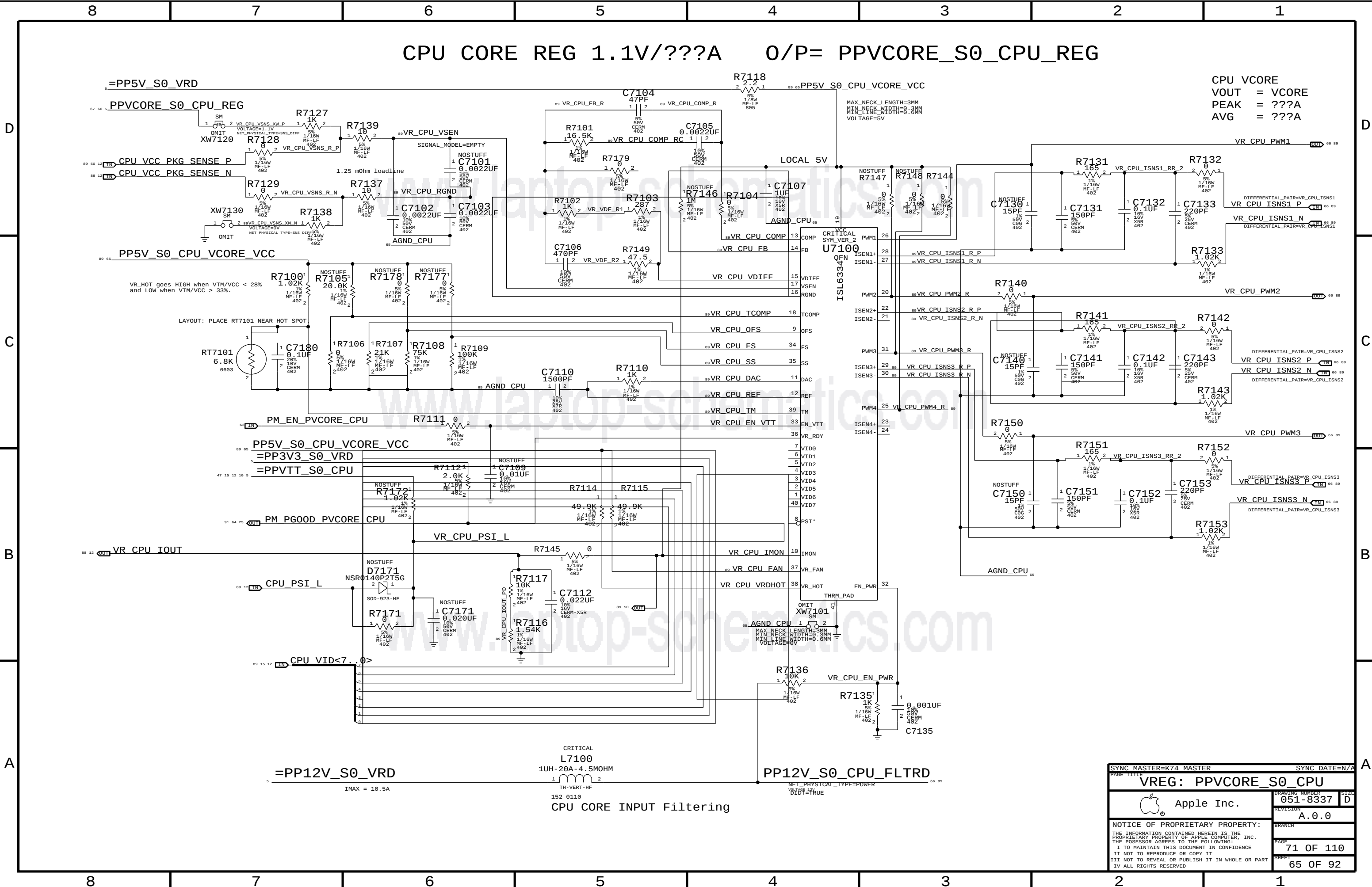


S0 RAILS PG00D



ALL_SYS_PWRGD CIRCUIT

PAGE TITLE		SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
POWER SEQUENCING PG00D		DRAWING NUMBER		SIZE	
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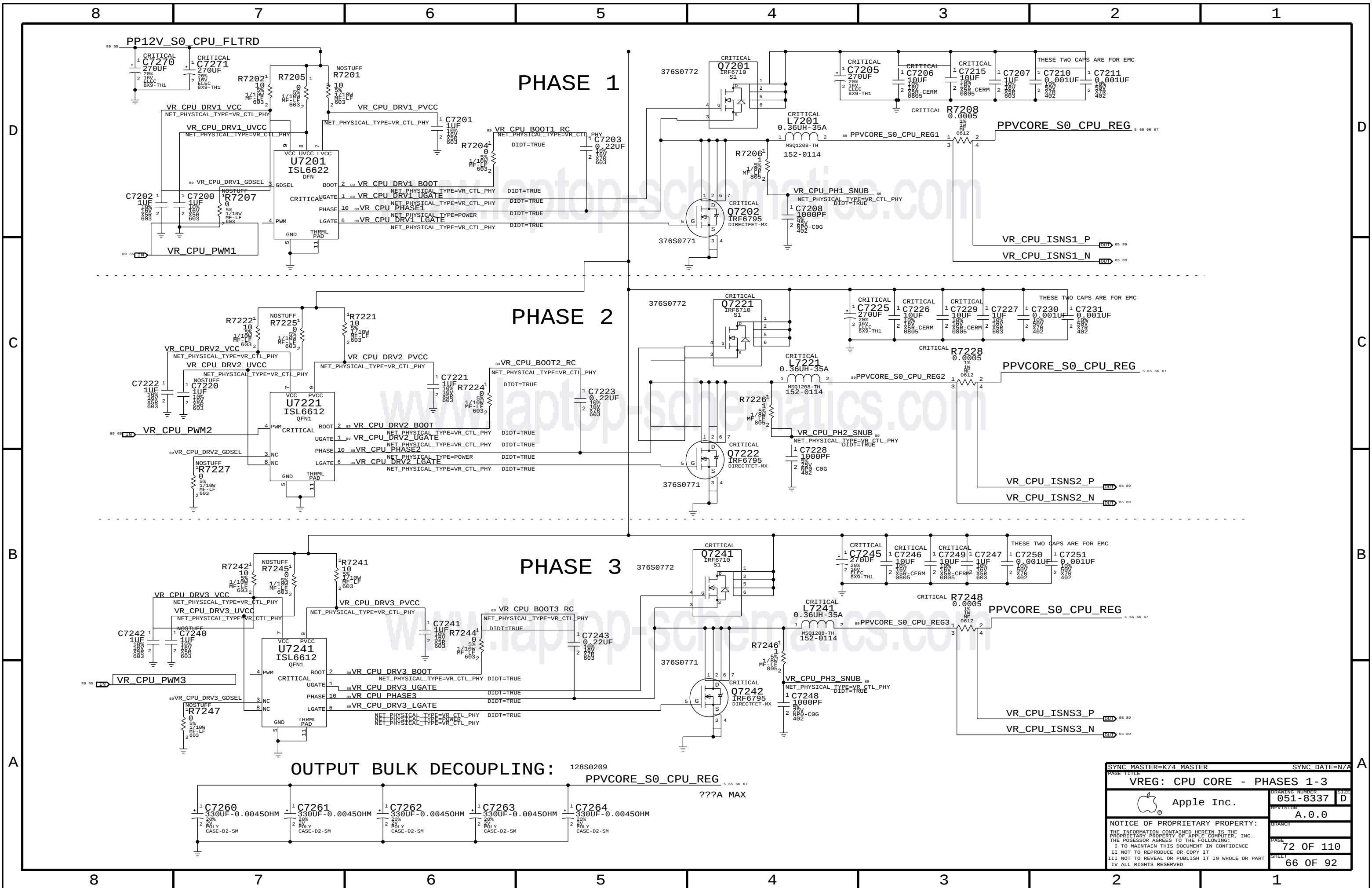


CPU CORE REG 1.1V/???A **O/P= PPVCORE_S0_CPU_REG**

CPU VCORE
VOUT = VCORE
PEAK = ???A
AVG = ???A

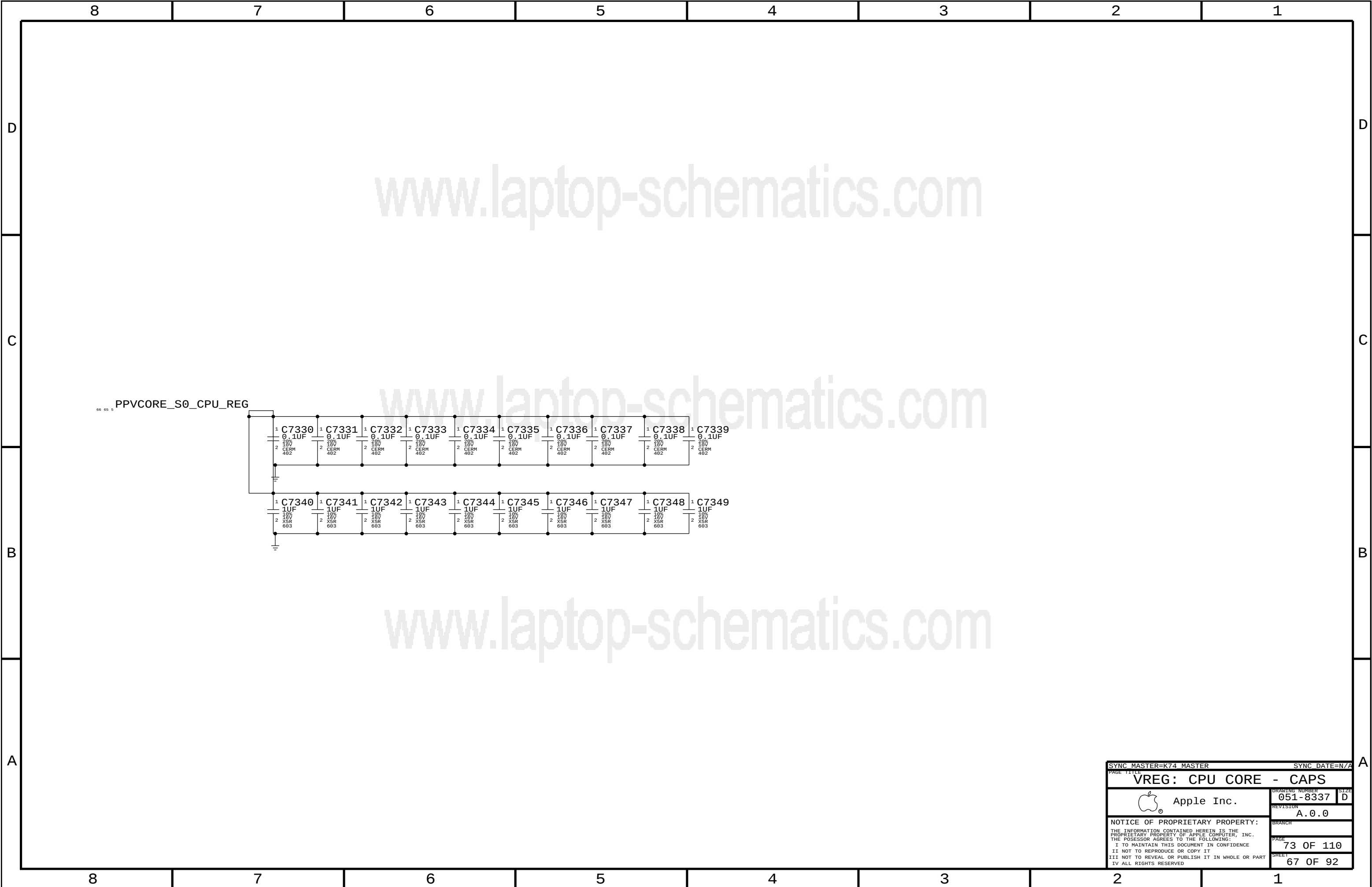
COMPONENTS:

- Resistors:** R7101, R7102, R7103, R7104, R7105, R7106, R7107, R7108, R7109, R7110, R7111, R7112, R7113, R7114, R7115, R7116, R7117, R7118, R7119, R7120, R7121, R7122, R7123, R7124, R7125, R7126, R7127, R7128, R7129, R7130, R7131, R7132, R7133, R7134, R7135, R7136, R7137, R7138, R7139, R7140, R7141, R7142, R7143, R7144, R7145, R7146, R7147, R7148, R7149, R7150, R7151, R7152, R7153, R7154, R7155, R7156, R7157, R7158, R7159, R7160, R7161, R7162, R7163, R7164, R7165, R7166, R7167, R7168, R7169, R7170, R7171, R7172, R7173, R7174, R7175, R7176, R7177, R7178, R7179, R7180, R7181, R7182, R7183, R7184, R7185, R7186, R7187, R7188, R7189, R7190, R7191, R7192, R7193, R7194, R7195, R7196, R7197, R7198, R7199, R7200, R7201, R7202, R7203, R7204, R7205, R7206, R7207, R7208, R7209, R7210, R7211, R7212, R7213, R7214, R7215, R7216, R7217, R7218, R7219, R7220, R7221, R7222, R7223, R7224, R7225, R7226, R7227, R7228, R7229, R7230, R7231, R7232, R7233, R7234, R7235, R7236, R7237, R7238, R7239, R7240, R7241, R7242, R7243, R7244, R7245, R7246, R7247, R7248, R7249, R7250, R7251, R7252, R7253, R7254, R7255, R7256, R7257, R7258, R7259, R7260, R7261, R7262, R7263, R7264, R7265, R7266, R7267, R7268, R7269, R7270, R7271, R7272, R7273, R7274, R7275, R7276, R7277, R7278, R7279, R7280, R7281, R7282, R7283, R7284, R7285, R7286, R7287, R7288, R7289, R7290, R7291, R7292, R7293, R7294, R7295, R7296, R7297, R7298, R7299, R7300, R7301, R7302, R7303, R7304, R7305, R7306, R7307, R7308, R7309, R7310, R7311, R7312, R7313, R7314, R7315, R7316, R7317, R7318, R7319, R7320, R7321, R7322, R7323, R7324, R7325, R7326, R7327, R7328, R7329, R7330, R7331, R7332, R7333, R7334, R7335, R7336, R7337, R7338, R7339, R7340, R7341, R7342, R7343, R7344, R7345, R7346, R7347, R7348, R7349, R7350, R7351, R7352, R7353, R7354, R7355, R7356, R7357, R7358, R7359, R7360, R7361, R7362, R7363, R7364, R7365, R7366, R7367, R7368, R7369, R7370, R7371, R7372, R7373, R7374, R7375, R7376, R7377, R7378, R7379, R7380, R7381, R7382, R7383, R7384, R7385, R7386, R7387, R7388, R7389, R7390, R7391, R7392, R7393, R7394, R7395, R7396, R7397, R7398, R7399, R7400, R7401, R7402, R7403, R7404, R7405, R7406, R7407, R7408, R7409, R7410, R7411, R7412, R7413, R7414, R7415, R7416, R7417, R7418, R7419, R7420, R7421, R7422, R7423, R7424, R7425, R7426, R7427, R7428, R7429, R7430, R7431, R7432, R7433, R7434, R7435, R7436, R7437, R7438, R7439, R7440, R7441, R7442, R7443, R7444, R7445, R7446, R7447, R7448, R7449, R7450, R7451, R7452, R7453, R7454, R7455, R7456, R7457, R7458, R7459, R7460, R7461, R7462, R7463, R7464, R7465, R7466, R7467, R7468, R7469, R7470, R7471, R7472, R7473, R7474, R7475, R7476, R7477, R7478, R7479, R7480, R7481, R7482, R7483, R7484, R7485, R7486, R7487, R7488, R7489, R7490, R7491, R7492, R7493, R7494, R7495, R7496, R7497, R7498, R7499, R7500, R7501, R7502, R7503, R7504, R7505, R7506, R7507, R7508, R7509, R7510, R7511, R7512, R7513, R7514, R7515, R7516, R7517, R7518, R7519, R7520, R7521, R7522, R7523, R7524, R7525, R7526, R7527, R7528, R7529, R7530, R7531, R7532, R7533, R7534, R7535, R7536, R7537, R7538, R7539, R7540, R7541, R7542, R7543, R7544, R7545, R7546, R7547, R7548, R7549, R7550, R7551, R7552, R7553, R7554, R7555, R7556, R7557, R7558, R7559, R7560, R7561, R7562, R7563, R7564, R7565, R7566, R7567, R7568, R7569, R7570, R7571, R7572, R7573, R7574, R7575, R7576, R7577, R7578, R7579, R7580, R7581, R7582, R7583, R7584, R7585, R7586, R7587, R7588, R7589, R7590, R7591, R7592, R7593, R7594, R7595, R7596, R7597, R7598, R7599, R7600, R7601, R7602, R7603, R7604, R7605, R7606, R7607, R7608, R7609, R7610, R7611, R7612, R7613, R7614, R7615, R7616, R7617, R7618, R7619, R7620, R7621, R7622, R7623, R7624, R7625, R7626, R7627, R7628, R7629, R7630, R7631, R7632, R7633, R7634, R7635, R7636, R7637, R7638, R7639, R7640, R7641, R7642, R7643, R7644, R7645, R7646, R7647, R7648, R7649, R7650, R7651, R7652, R7653, R7654, R7655, R7656, R7657, R7658, R7659, R7660, R7661, R7662, R7663, R7664, R7665, R7666, R7667, R7668, R7669, R7670, R7671, R7672, R7673, R7674, R7675, R7676, R7677, R7678, R7679, R7680, R7681, R7682, R7683, R7684, R7685, R7686, R7687, R7688, R7689, R7690, R7691, R7692, R7693, R7694, R7695, R7696, R7697, R7698, R7699, R7700, R7701, R7702, R7703, R7704, R7705, R7706, R7707, R7708, R7709, R7710, R7711, R7712, R7713, R7714, R7715, R7716, R7717, R7718, R7719, R7720, R7721, R7722, R7723, R7724, R7725, R7726, R7727, R7728, R7729, R7730, R7731, R7732, R7733, R7734, R7735, R7736, R7737, R7738, R7739, R7740, R7741, R7742, R7743, R7744, R7745, R7746, R7747, R7748, R7749, R7750, R7751, R7752, R7753, R7754, R7755, R7756, R7757, R77



OUTPUT BULK DECOUPLING: 128S0209
PPVCORE_S0_CPU_REG
???A MAX

SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE		VREG: CPU CORE - PHASES 1-3	
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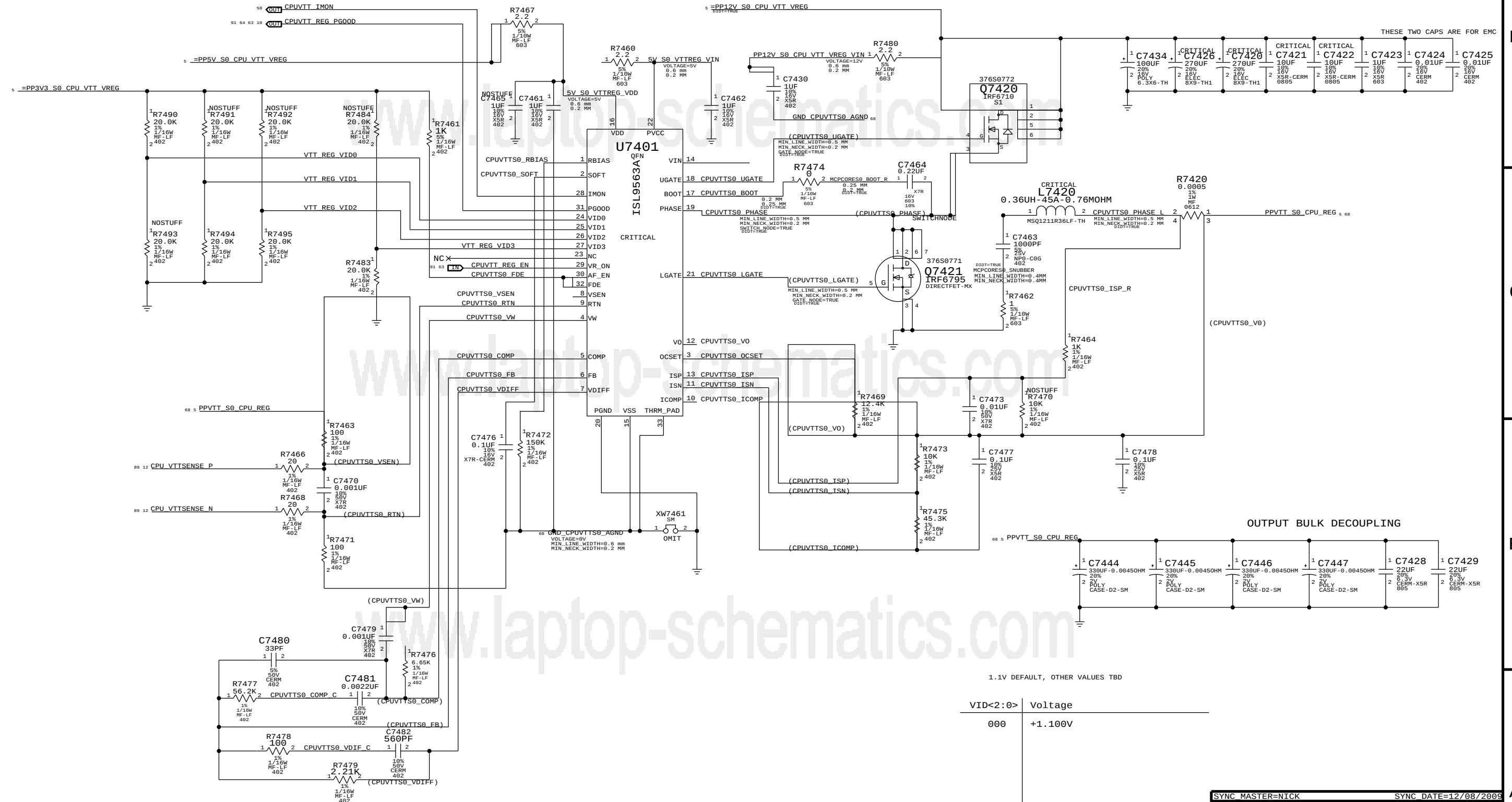


SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE		VREG: CPU CORE - CAPS	
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CPU VTT REG 1.1V

0/P= PPVTT_S0_CPU_REG



1.1V DEFAULT, OTHER VALUES TBD

VID<2:0>	Voltage
000	+1.100V

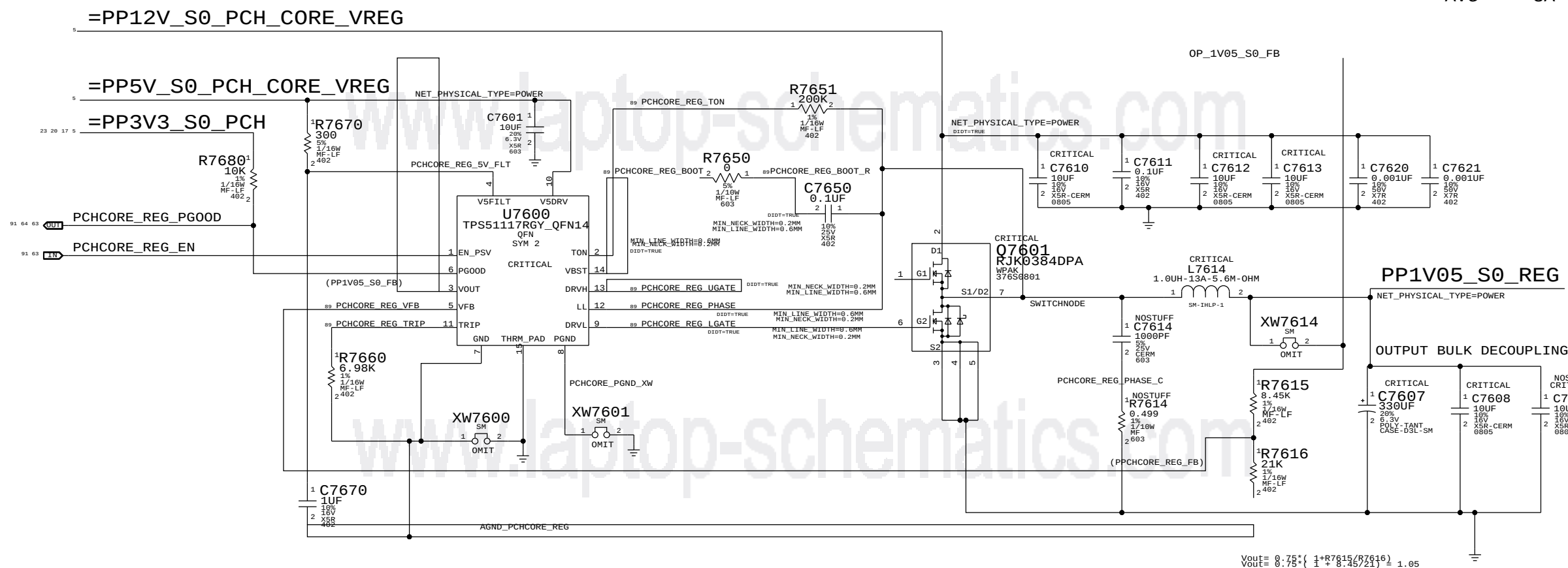
SYNC MASTER-NICK		SYNC DATE=12/08/2009	
PAGE TITLE			
CPU VTT REGULATOR			
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		SIZE D	
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		SHEET 68 OF 92	

IBEX PEAK CORE REG 1.05V OUTPUT = PP1V05_S0_REG

PP1V05_S0_REG

$$V_{OUT} = 1.05V$$

PEAK = 7.5A

$$AVG = 3A$$

$$V_{out} = 0.75 * \left(\frac{1 + R_{7615}/R_{7616}}{1 + 8.45/21} \right) = 1.0$$

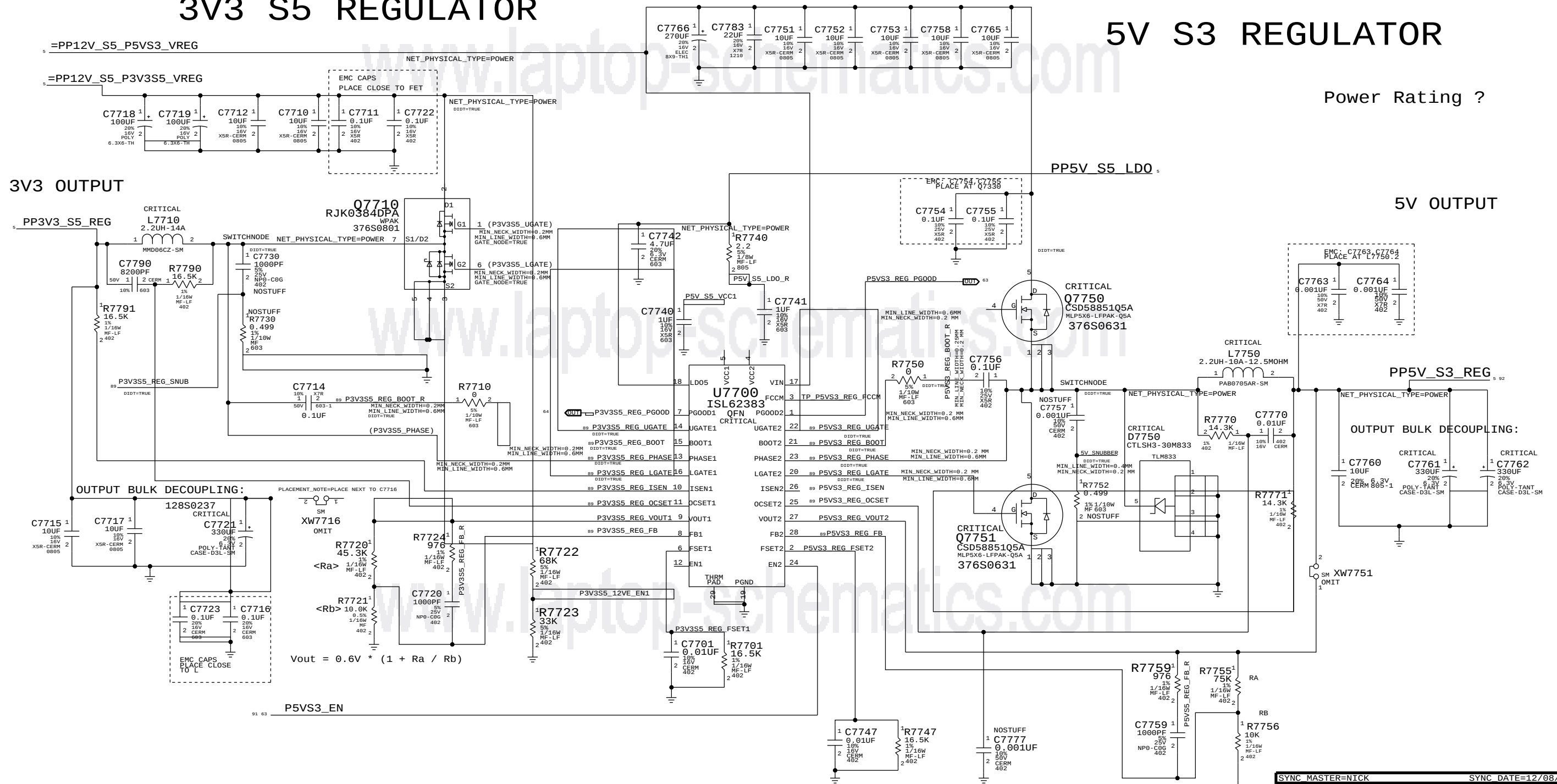
3V3 S5 REGULATOR

5V S3 REGULATOR

Power Rating ?

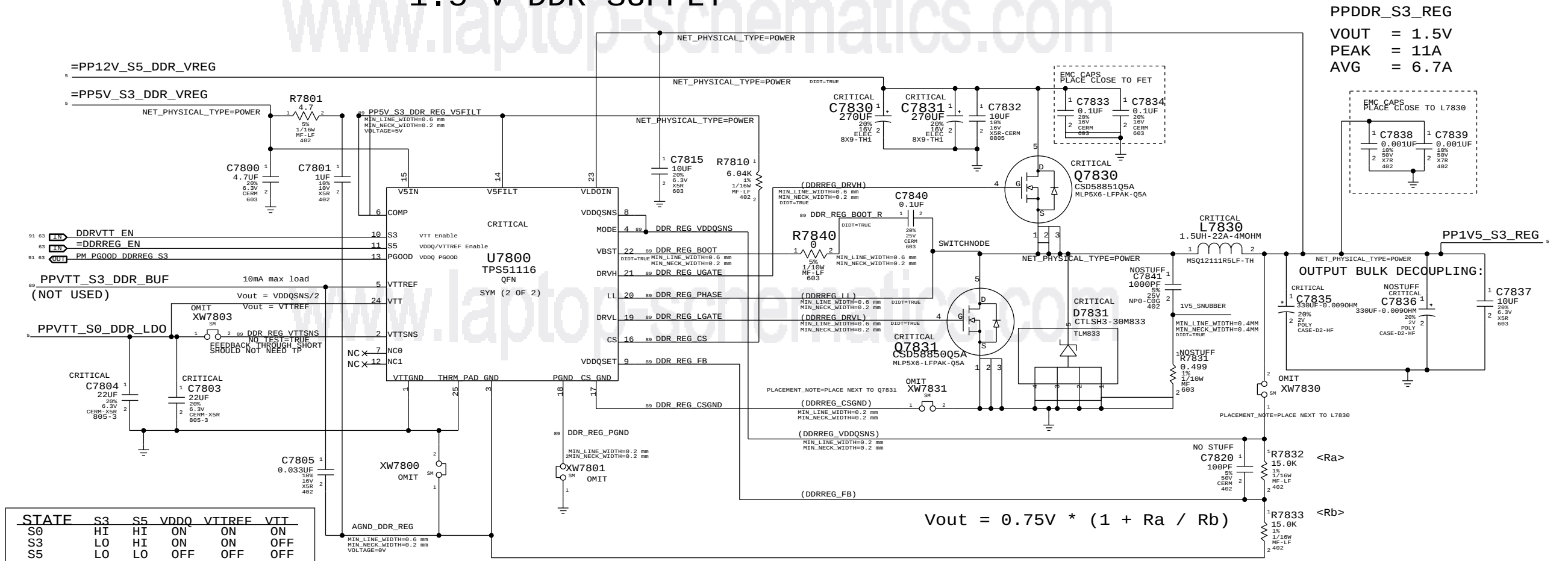
5V OUTPUT

3V3 OUTPUT

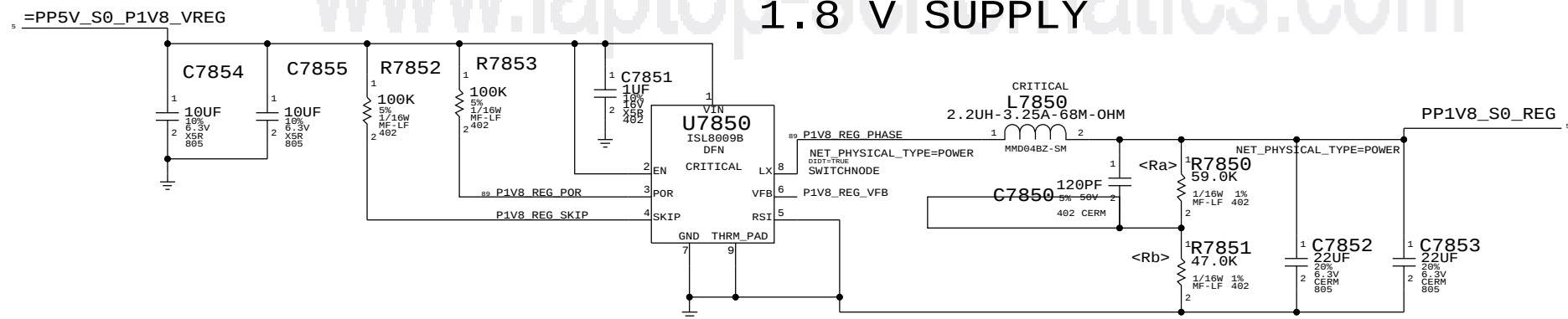


SYNC MASTER=NICK		SYNC DATE=12/08/2009	
PAGE TITLE			
5V_S3 / 3V3_S5		VREGS	
		DRAWING NUMBER	051-8337
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1.5 V DDR SUPPLY



1.8 V SUPPLY



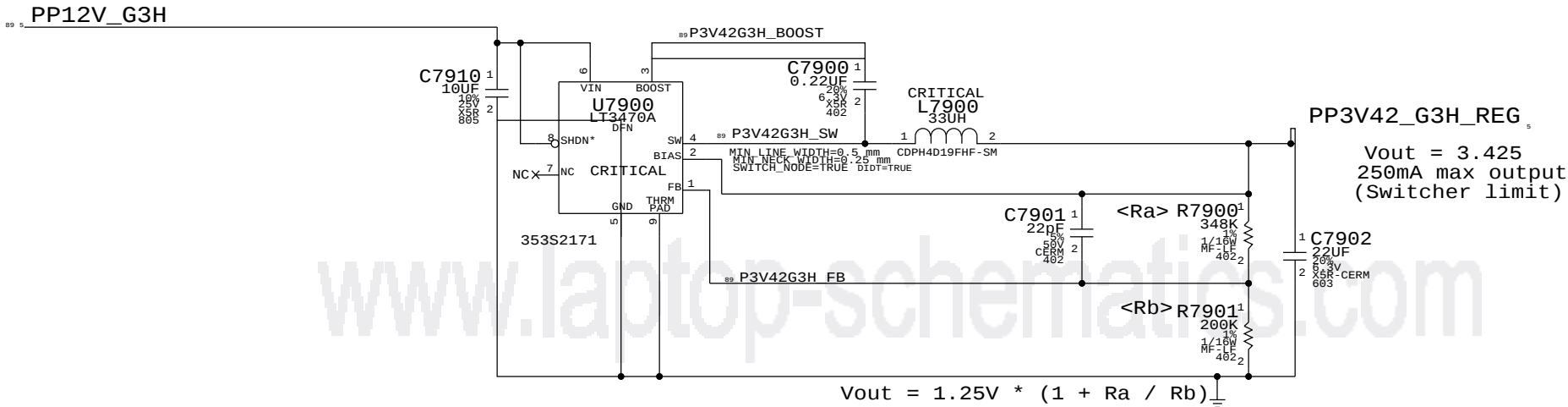
$$V_o = 0.8 * (1 + R_a / R_b)$$

$$V_o = 0.8 * (1 + 59 / 47) = 1.804V$$

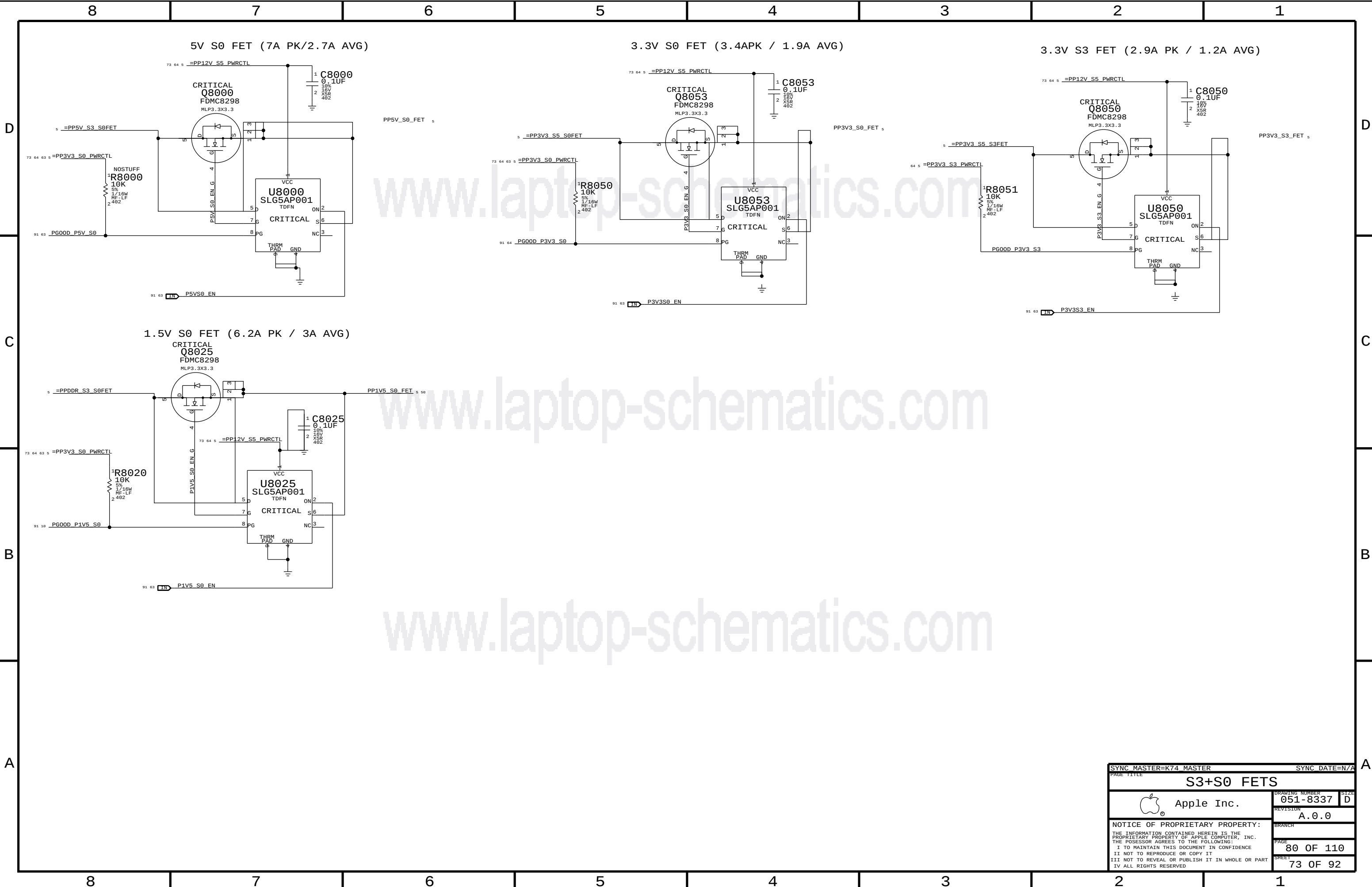
SYNC MASTER=K23F		SYNC DATE=11/30/2009	
PAGE TITLE		1.5V / 1.8V VREGS	
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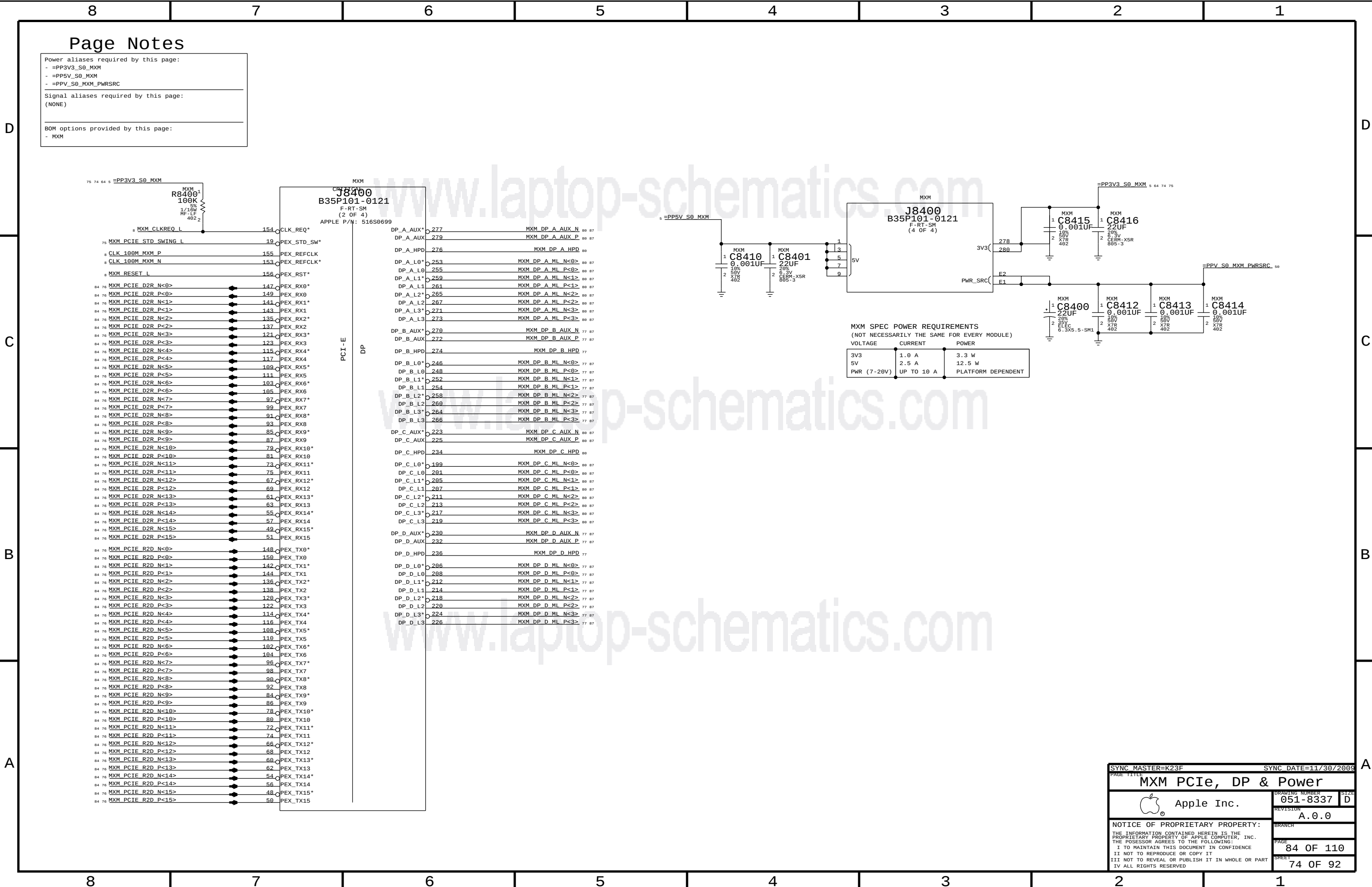
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE		3.42 G3HOT SUPPLY	
DRAWING NUMBER		051-8337	SIZE D
REVISION		A.0.0	BRANCH
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Page Notes

Power aliases required by this page:

- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

- MXM

MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

SYNC MASTER=K23F SYNC DATE=11/30/2009

PAGE TITLE

MXM PCIe, DP & Power



Apple Inc.

DRAWING NUMBER

051-8337

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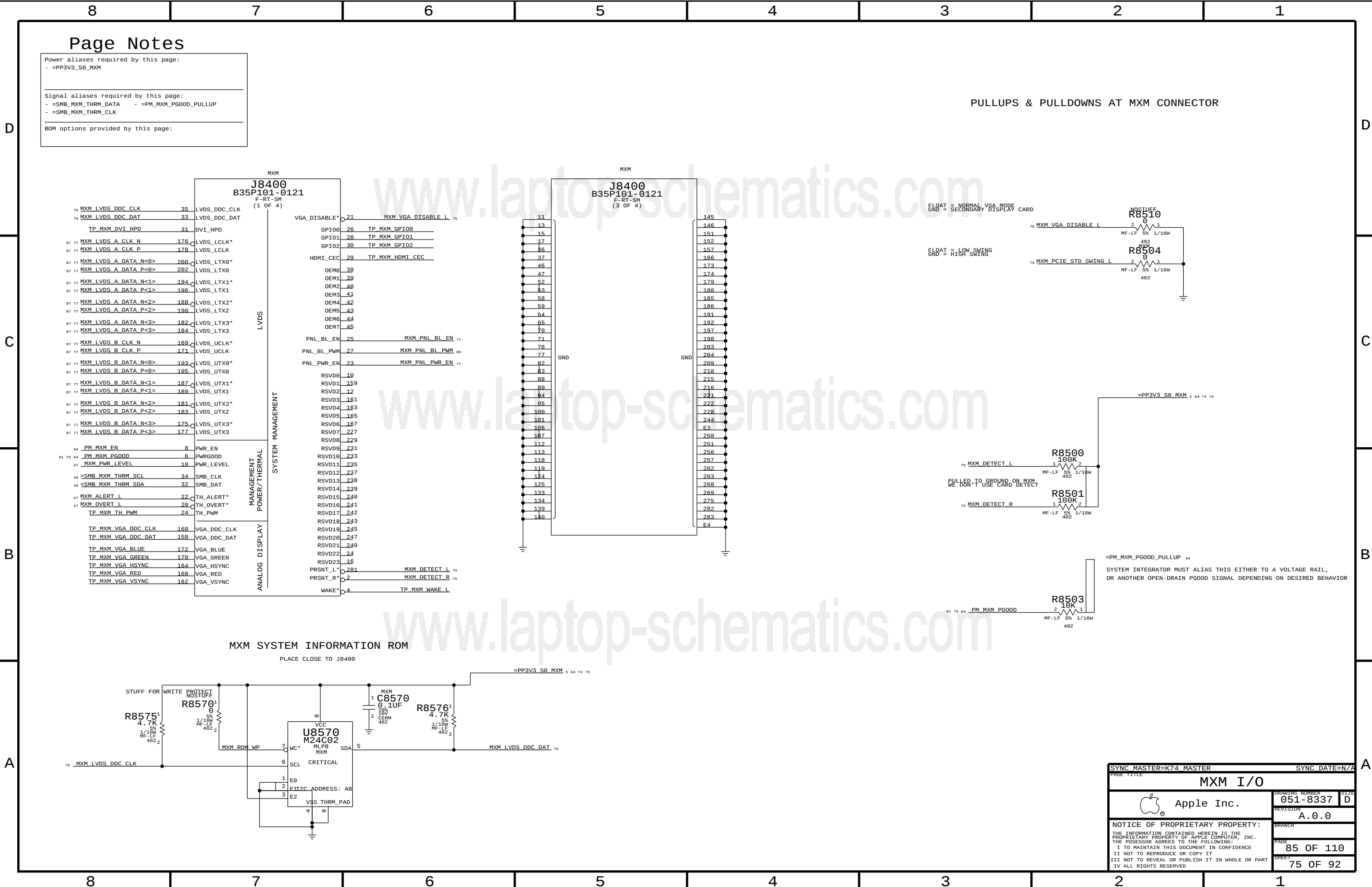
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PAGE

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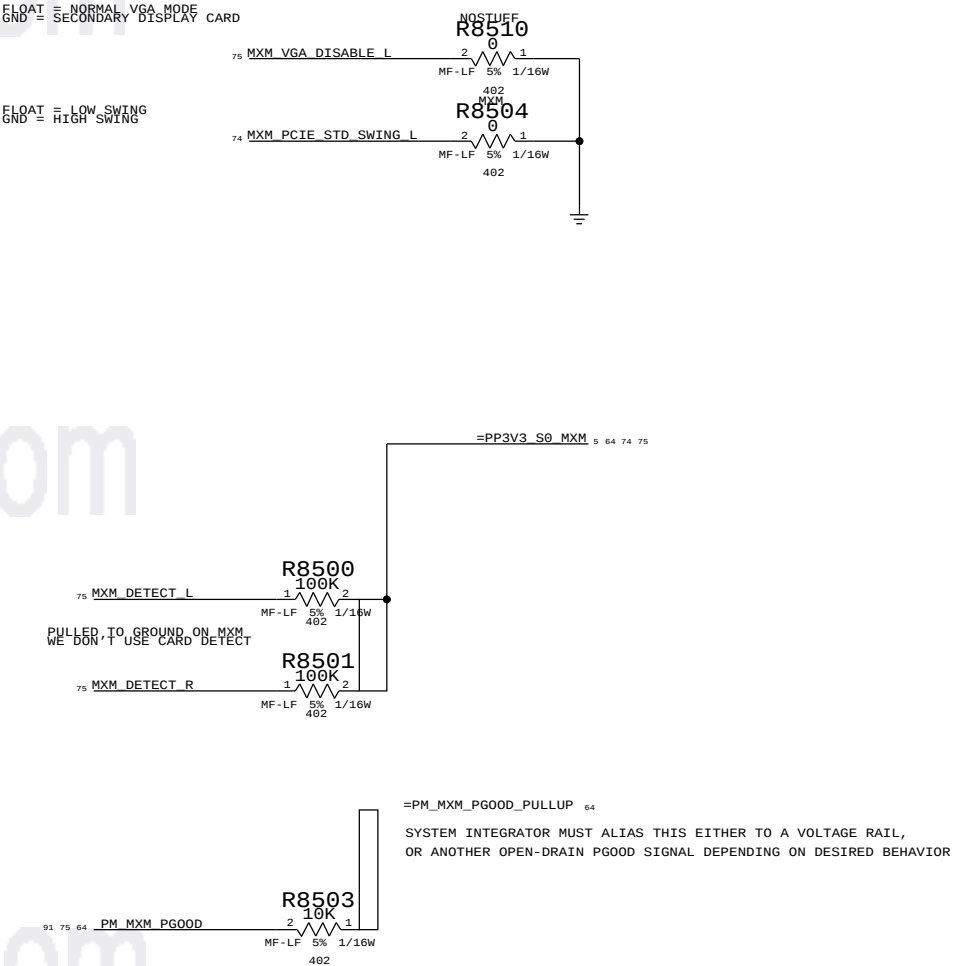
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA - =PM_MXM_PG00D_PULLUP
- =SMB_MXM_THRM_CLK

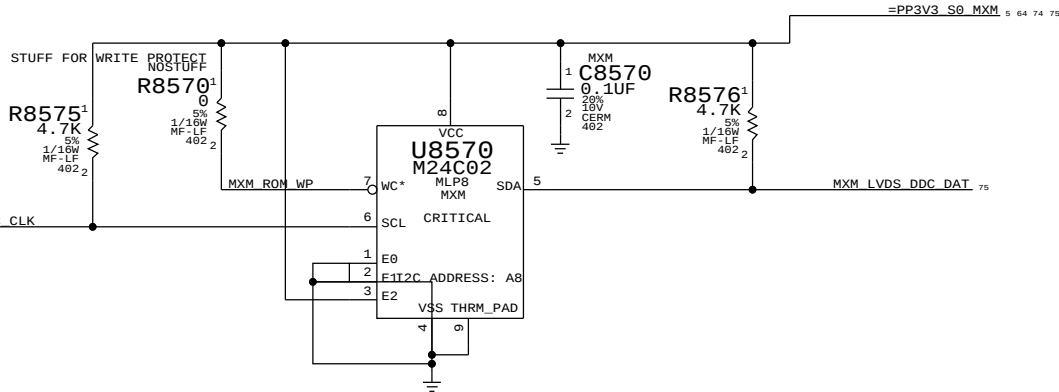
BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR



MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



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MXM I/O		DRAWING NUMBER	
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Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Unused MXM Interfaces

87 75	MXM LVDS A CLK N	==	NC MXM LVDS A CLK N	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS A CLK P	==	NC MXM LVDS A CLK P	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS A DATA N<0>	==	NC MXM LVDS A DATA N<0>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS A DATA P<0>	==	NC MXM LVDS A DATA P<0>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS A DATA N<1>	==	NC MXM LVDS A DATA N<1>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS A DATA P<1>	==	NC MXM LVDS A DATA P<1>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS A DATA N<2>	==	NC MXM LVDS A DATA N<2>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS A DATA P<2>	==	NC MXM LVDS A DATA P<2>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS A DATA N<3>	==	NC MXM LVDS A DATA N<3>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS A DATA P<3>	==	NC MXM LVDS A DATA P<3>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS B CLK N	==	NC MXM LVDS B CLK N	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS B CLK P	==	NC MXM LVDS B CLK P	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS B DATA N<0>	==	NC MXM LVDS B DATA N<0>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS B DATA P<0>	==	NC MXM LVDS B DATA P<0>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS B DATA N<1>	==	NC MXM LVDS B DATA N<1>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS B DATA P<1>	==	NC MXM LVDS B DATA P<1>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS B DATA N<2>	==	NC MXM LVDS B DATA N<2>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS B DATA P<2>	==	NC MXM LVDS B DATA P<2>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS B DATA N<3>	==	NC MXM LVDS B DATA N<3>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM LVDS B DATA P<3>	==	NC MXM LVDS B DATA P<3>	==	MAKE_BASE=TRUE NO_TEST=TRUE

Unused MXM DP Interfaces

87 74	MXM DP B MI P<0..3>	==	NC MXM DP B MI P<0..3>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM DP B MI N<0..3>	==	NC MXM DP B MI N<0..3>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM DP B AUX P	==	NC MXM DP B AUX P	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM DP B AUX N	==	NC MXM DP B AUX N	==	MAKE_BASE=TRUE NO_TEST=TRUE
74	MXM DP B HPD	==	NC MXM DP B HPD	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM DP D MI P<0..3>	==	NC MXM DP D MI P<0..3>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM DP D MI N<0..3>	==	NC MXM DP D MI N<0..3>	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM DP D AUX P	==	NC MXM DP D AUX P	==	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM DP D AUX N	==	NC MXM DP D AUX N	==	MAKE_BASE=TRUE NO_TEST=TRUE
74	MXM DP D HPD	==	NC MXM DP D HPD	==	MAKE_BASE=TRUE NO_TEST=TRUE

UNUSED MXM CONTROL SIGNALS

75	MXM PNL BL EN	==	NC MXM PNL BL EN	==	MAKE_BASE=TRUE NO_TEST=TRUE
75	MXM PNL PWR EN	==	NC MXM PNL PWR EN	==	MAKE_BASE=TRUE NO_TEST=TRUE

DISPLAY AUDIO MUX NOT USED - SEND SPDIF TO CODEC

85 60	TPN	AUD SPDIF IN	==	AUD SPDIF IN CODEC	OUT	56
		MAKE_BASE=TRUE				
78	TPN	DP INT SPDIF AUDIO	==	TP DP INT SPDIF AUDIO		
		MAKE_BASE=TRUE				

SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE			
Display: Aliases			
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		REVISION	A.0.0
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Page Notes

Power aliases required by this page:

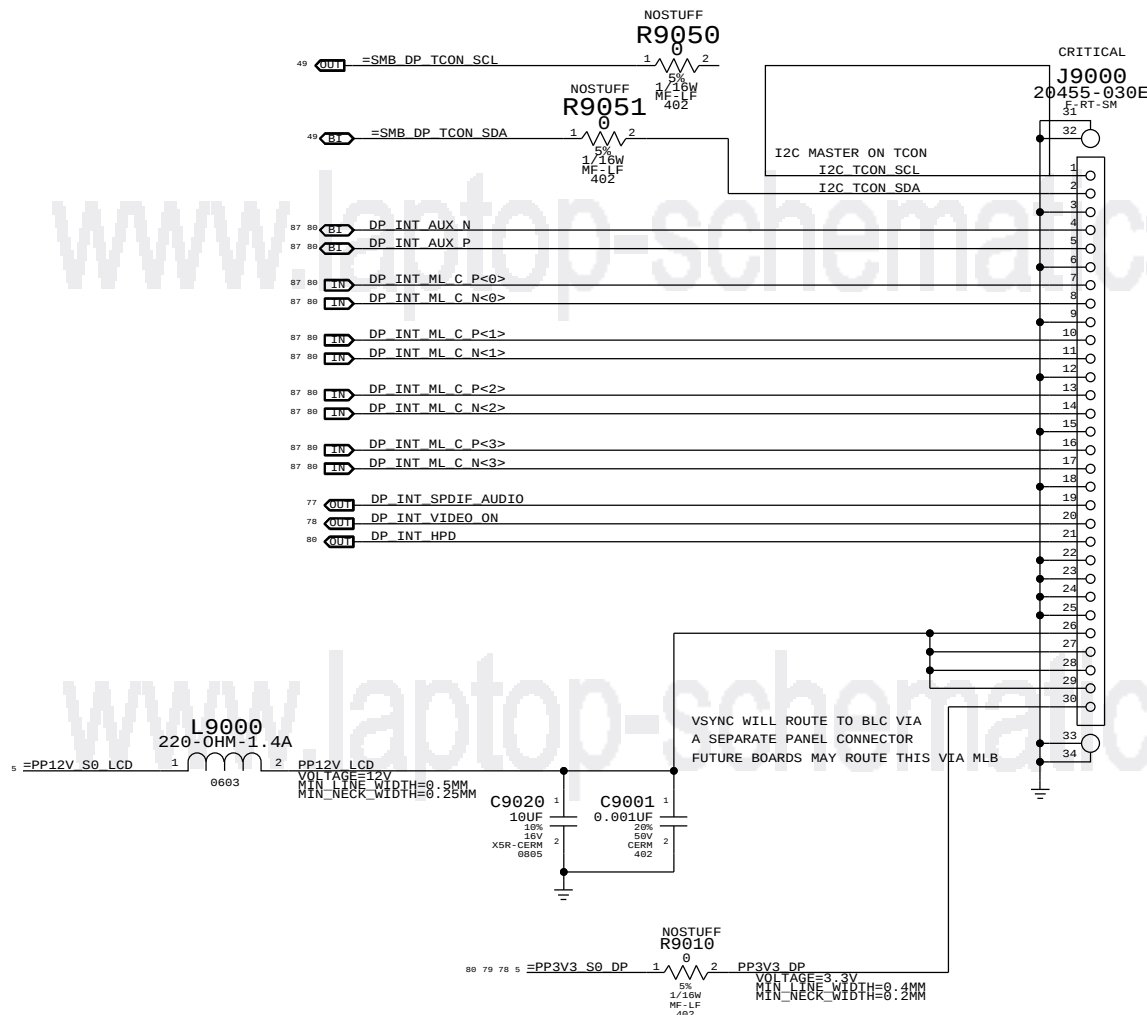
- =PP12V_S0_LCD
- =PP3V3_S0_DP

Signal aliases required by this page:

- =SMB_DP_TCON_SCL, =SMB_DP_TCON_SDA

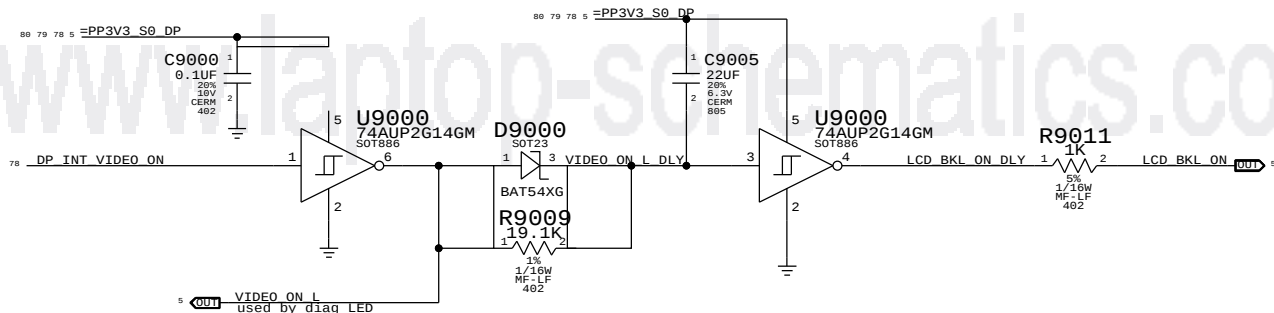
BOM options provided by this page:

INTERNAL DP INTERFACE

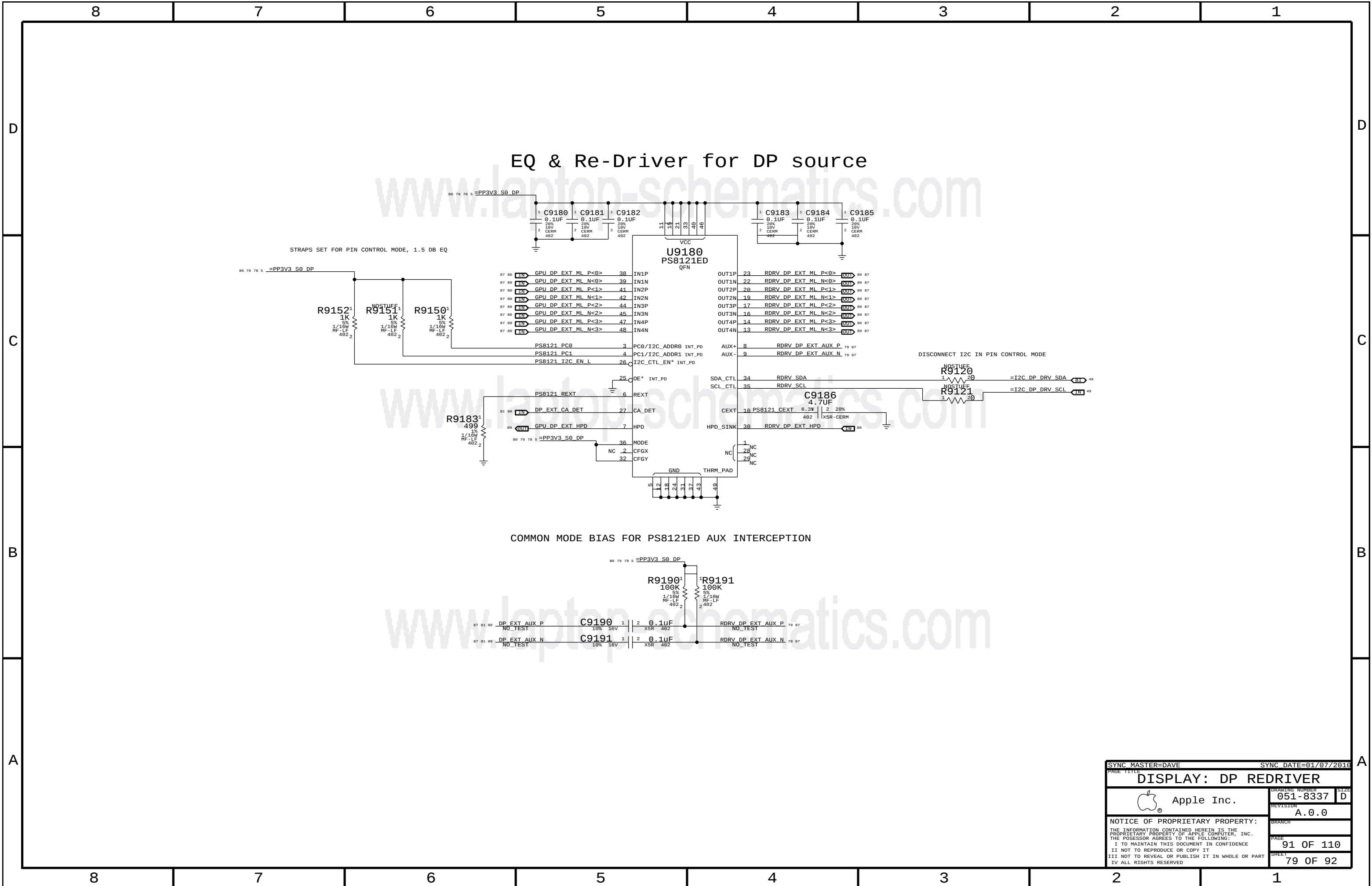


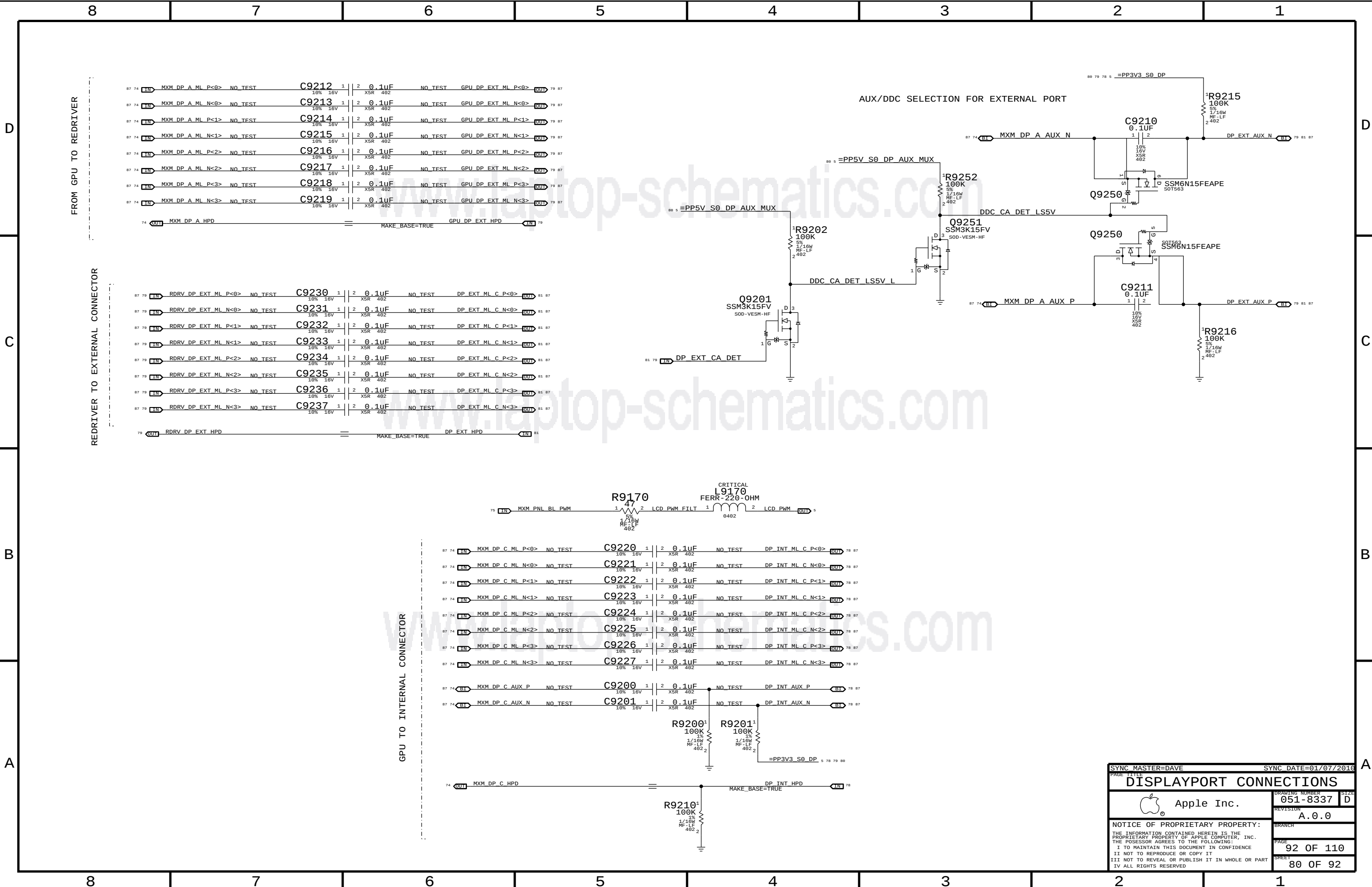
BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video



PAGE 12/12		SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
Display: Int DP Connector		DRAWING NUMBER		SIZE	
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D

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B

A

Need to support MEM_*-style wildcards!

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_RCOMP	*	0.2 MM	?



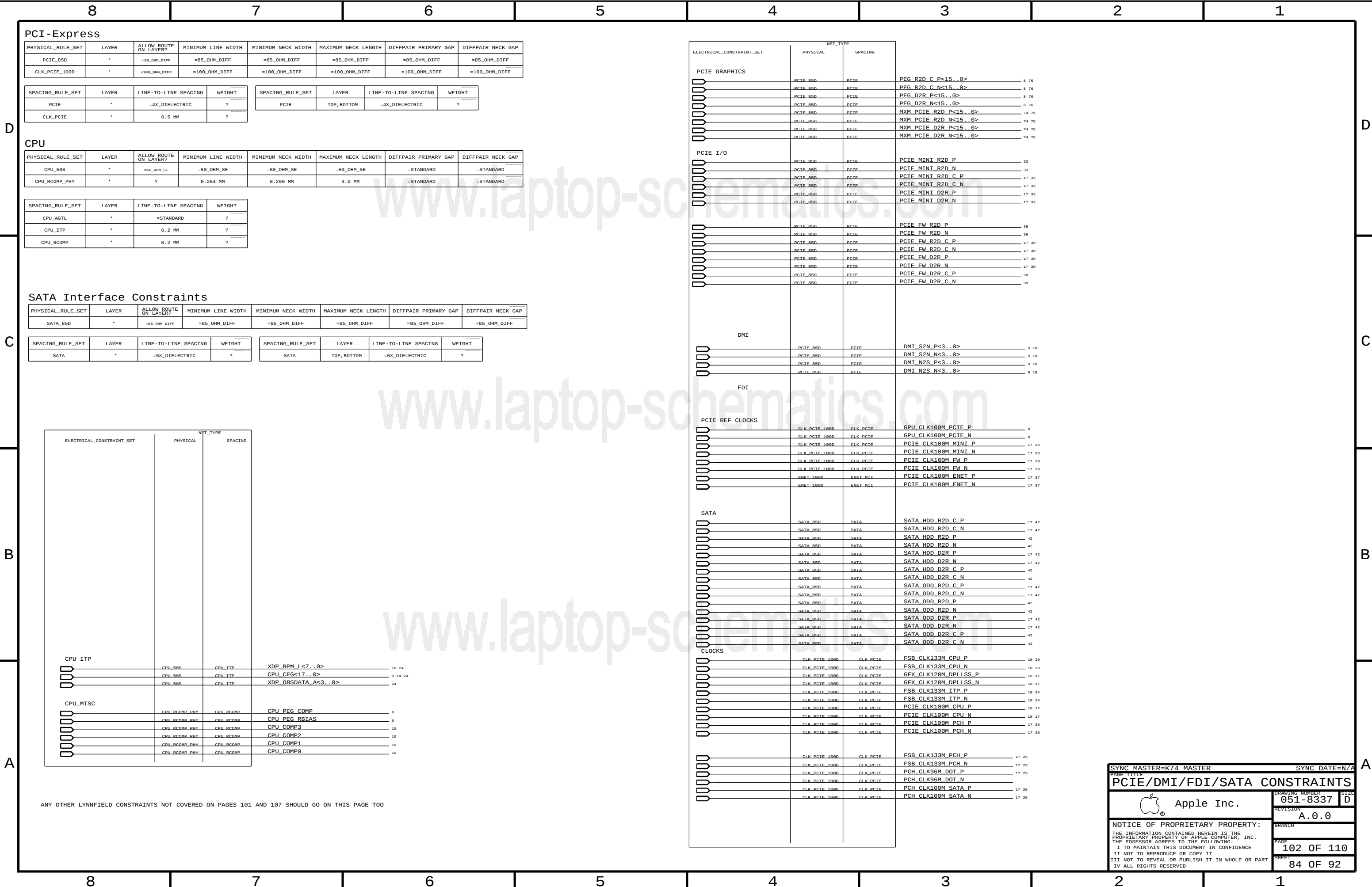
D

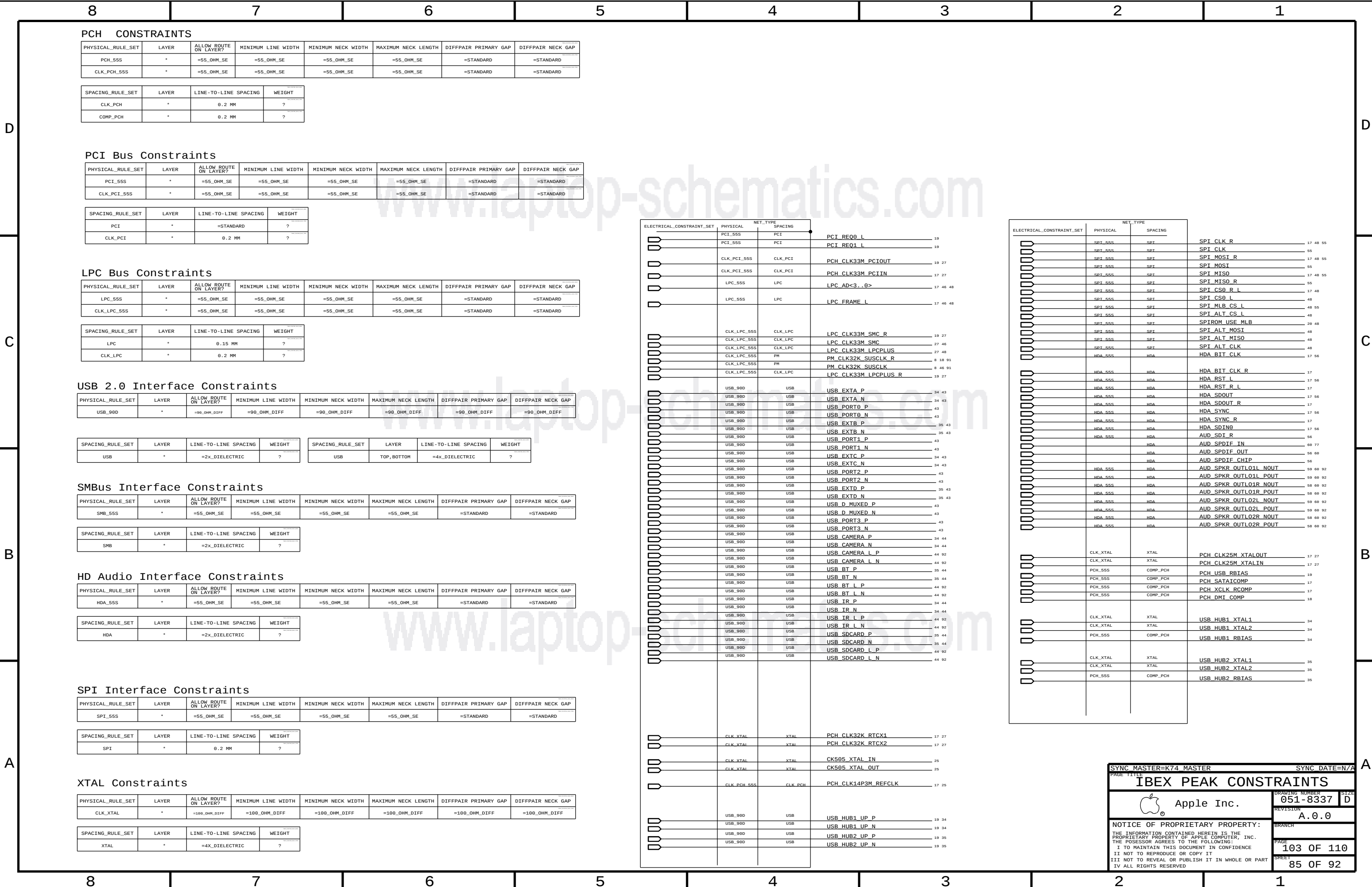
C

B

A

SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE			
Memory Constraints			
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		SIZE	D
		REVISION	A.0.0
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PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
CLK_PCH	*	0.2 MM	?
COMP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
USB	*	=2X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
USB	TOP,BOTTOM	=4X_DIELECTRIC	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
SMB	*	=2X_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
HDA	*	=2X_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
SPI	*	0.2 MM	?

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
	PCI_55S	PCI	PCI REQ0 L 19
	PCI_55S	PCI	PCI REQ1 L 19
	CLK_PCI_55S	CLK_PCI	PCH CLK33M PCIOUT 19 27
	CLK_PCI_55S	CLK_PCI	PCH CLK33M PCIIN 17 27
	LPC_55S	LPC	LPC AD<3..0> 17 46 48
	LPC_55S	LPC	LPC FRAME L 17 46 48
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC R 19 27
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC 27 46
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS 27 48
	CLK_LPC_55S	PM	PM CLK32K SUSCLK R 8 18 91
	CLK_LPC_55S	PM	PM CLK32K SUSCLK 8 46 91
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS R 19 27
	USB_90D	USB	USB EXTA P 34 43
	USB_90D	USB	USB EXTA N 34 43
	USB_90D	USB	USB PORT0 P 43
	USB_90D	USB	USB PORT0 N 43
	USB_90D	USB	USB EXTB P 35 43
	USB_90D	USB	USB EXTB N 35 43
	USB_90D	USB	USB PORT1 P 43
	USB_90D	USB	USB PORT1 N 43
	USB_90D	USB	USB EXTC P 34 43
	USB_90D	USB	USB EXTC N 34 43
	USB_90D	USB	USB PORT2 P 43
	USB_90D	USB	USB PORT2 N 43
	USB_90D	USB	USB EXTD P 35 43
	USB_90D	USB	USB EXTD N 35 43
	USB_90D	USB	USB D MUXED P 43
	USB_90D	USB	USB D MUXED N 43
	USB_90D	USB	USB PORT3 P 43
	USB_90D	USB	USB PORT3 N 43
	USB_90D	USB	USB CAMERA P 34 44
	USB_90D	USB	USB CAMERA N 34 44
	USB_90D	USB	USB CAMERA L P 44 92
	USB_90D	USB	USB CAMERA L N 44 92
	USB_90D	USB	USB BT P 35 44
	USB_90D	USB	USB BT N 35 44
	USB_90D	USB	USB BT L P 44 92
	USB_90D	USB	USB BT L N 44 92
	USB_90D	USB	USB IR P 34 44
	USB_90D	USB	USB IR N 34 44
	USB_90D	USB	USB IR L P 44 92
	USB_90D	USB	USB IR L N 44 92
	USB_90D	USB	USB SDCARD P 35 44
	USB_90D	USB	USB SDCARD N 35 44
	USB_90D	USB	USB SDCARD L P 44 92
	USB_90D	USB	USB SDCARD L N 44 92
	CLK_XTAL	XTAL	PCH CLK32K RTCX1 17 27
	CLK_XTAL	XTAL	PCH CLK32K RTCX2 17 27
	CLK_XTAL	XTAL	CK505 XTAL IN 25
	CLK_XTAL	XTAL	CK505 XTAL OUT 25
	CLK_PCH_55S	CLK_PCH	PCH CLK14P3M REFCLK 17 25
	USB_90D	USB	USB HUB1 UP P 19 34
	USB_90D	USB	USB HUB1 UP N 19 34
	USB_90D	USB	USB HUB2 UP P 19 35
	USB_90D	USB	USB HUB2 UP N 19 35

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
	SPI_55S	SPI	SPI CLK R 17 48 55
	SPI_55S	SPI	SPI CLK 55
	SPI_55S	SPI	SPI MOSI R 17 48 55
	SPI_55S	SPI	SPI MOSI 55
	SPI_55S	SPI	SPI MISO 17 48 55
	SPI_55S	SPI	SPI MISO R 55
	SPI_55S	SPI	SPI CS0 R L 17 48
	SPI_55S	SPI	SPI CS0 L 48
	SPI_55S	SPI	SPI MLB CS L 48 55
	SPI_55S	SPI	SPI ALT CS L 48
	SPI_55S	SPI	SPI ALT CS L 48 55
	SPI_55S	SPI	SPI ALT MOSI 28 48
	SPI_55S	SPI	SPI ALT MOSI 48
	SPI_55S	SPI	SPI ALT MISO 48
	SPI_55S	SPI	SPI ALT CLK 48
	HDA_55S	HDA	HDA BIT CLK 17 56
	HDA_55S	HDA	HDA BIT CLK R 17
	HDA_55S	HDA	HDA RST L 17 56
	HDA_55S	HDA	HDA RST R L 17
	HDA_55S	HDA	HDA SDOOUT 17 56
	HDA_55S	HDA	HDA SDOOUT R 17
	HDA_55S	HDA	HDA SYNC 17 56
	HDA_55S	HDA	HDA SYNC R 17
	HDA_55S	HDA	HDA SDIN0 17 56
	HDA_55S	HDA	AUD SDI R 56
	HDA_55S	HDA	AUD SPDIF IN 66 77
	HDA_55S	HDA	AUD SPDIF OUT 56 66
	HDA_55S	HDA	AUD SPDIF CHIP 56
	HDA_55S	HDA	AUD SPKR OUTL01L NOUT 59 66 92
	HDA_55S	HDA	AUD SPKR OUTL01L POUT 59 66 92
	HDA_55S	HDA	AUD SPKR OUTL01R NOUT 59 66 92
	HDA_55S	HDA	AUD SPKR OUTL01R POUT 59 66 92
	HDA_55S	HDA	AUD SPKR OUTL02L NOUT 59 66 92
	HDA_55S	HDA	AUD SPKR OUTL02L POUT 59 66 92
	HDA_55S	HDA	AUD SPKR OUTL02R NOUT 59 66 92
	HDA_55S	HDA	AUD SPKR OUTL02R POUT 59 66 92
	CLK_XTAL	XTAL	PCH CLK25M XTALOUT 17 27
	CLK_XTAL	XTAL	PCH CLK25M XTALIN 17 27
	PCH_55S	COMP_PCH	PCH USB RBIAS 19
	PCH_55S	COMP_PCH	PCH SATAICOMP 17
	PCH_55S	COMP_PCH	PCH XCLK RCOMP 17
	PCH_55S	COMP_PCH	PCH DMI COMP 18
	CLK_XTAL	XTAL	USB HUB1 XTAL1 34
	CLK_XTAL	XTAL	USB HUB1 XTAL2 34
	PCH_55S	COMP_PCH	USB HUB1 RBIAS 34
	CLK_XTAL	XTAL	USB HUB2 XTAL1 35
	CLK_XTAL	XTAL	USB HUB2 XTAL2 35
	PCH_55S	COMP_PCH	USB HUB2 RBIAS 35

PAGE TITLE		SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
IBEX PEAK CONSTRAINTS		DRAWING NUMBER		SIZE	
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CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?
ENET_SE	*	=STANDARD	?

SOURCE: BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF	*	0.6 MM	?

CAESAR IV (SD) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD	*	=3:1 SPACING	?

FireWire Interface Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

AUDIO CONSTRAINTS

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UNDEF	0	0.1 SPACES	0

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUD_DIFF	*	1:1_DIFFPAIR

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPLICING
	ENET 50S	ENET SE	
	ENET 50S	BUE0 CLK	
	ENET 50S	BUE0 CLK	
	ENET 50S	BUE0 CLK	
	ENET 100D	ENET DIFF	
	ENET 100D	ENET DIFF	
	ENET 100D	ENET DIFF	
	ENET 100D	ENET DIFF	
	ENET 100D	ENET MIT	
	ENET 100D	ENET MIT	
	ENET 100D	ENET MIT	
	ENET 100D	ENET MIT	
	ENET 100D	ENET MIT	
	ENET 100D	ENET MIT	
	ENET 100D	ENET MIT	
	ENET 100D	ENET MIT	
	SD 50S	SD	
	SD 50S	SD	
	SD 50S	SD	
	SD 50S	SD	
	SD 50S	SD	

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
	PHYSICAL	SPACING		
	FW_1100	FW_TP	FW_PORT0_TPA_P	40
	FW_1100	FW_TP	FW_PORT0_TPA_N	40
	FW_1100	FW_TP	FW_PORT0_TPB_P	40
	FW_1100	FW_TP	FW_PORT0_TPB_N	40
	FW_1100	FW_TP	FW_PORT0_TPA_F_P	41
	FW_1100	FW_TP	FW_PORT0_TPA_F_N	41
	FW_1100	FW_TP	FW_PORT0_TPB_F_P	41
	FW_1100	FW_TP	FW_PORT0_TPB_F_N	41
PORT 1 & 2 NOT USED				
	FW_1100	FW_TP	FW_P0_TPA_L_P	40
	FW_1100	FW_TP	FW_P0_TPA_L_N	40
	FW_1100	FW_TP	FW_P0_TPB_L_P	40
	FW_1100	FW_TP	FW_P0_TPB_L_N	40
UNUSED FW NETS PHYSICAL PROPERTIES				
	FW_1100	FW_TP	FW_P1_TPA_P	39
	FW_1100	FW_TP	FW_P1_TPA_N	39
	FW_1100	FW_TP	FW_P2_TPA_P	39
	FW_1100	FW_TP	FW_P2_TPA_N	39 40

AUDIO NET PROPERTIES

[illegible]

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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
		SMR 55S	SMR	SMBUS_SMC_A_S3_SCL	49
		SMR 55S	SMR	SMBUS_SMC_A_S3_SDA	49
		SMR 55S	SMR	SMBUS_SMC_B_S0_SCL	49
		SMR 55S	SMR	SMBUS_SMC_B_S0_SDA	49
		SMR 55S	SMR	SMBUS_SMC_0_S0_SCL	49
		SMR 55S	SMR	SMBUS_SMC_0_S0_SDA	49
		SMR 55S	SMR	SMBUS_SMC_BSA_SCL	49
		SMR 55S	SMR	SMBUS_SMC_BSA_SDA	49
		SMR 55S	SMR	SMBUS_SMC_MGMT_SCL	49
		SMR 55S	SMR	SMBUS_SMC_MGMT_SDA	49
		SMR 55S	SMR	SMBUS_SMC_MGMT_SCL	49
		SMR 55S	SMR	SMBUS_SMC_MGMT_SDA	49
		SMR 55S	SMR	SMBUS_PCH_CLK	17
		SMR 55S	SMR	SMBUS_PCH_DATA	17
		SMR 55S	SMR	SML_PCH_0_CLK	17
		SMR 55S	SMR	SML_PCH_0_DATA	17
		SMR 55S	SMR	SML_PCH_1_CLK	17
		SMR 55S	SMR	SML_PCH_1_DATA	17
		CLK_XTAL	XTAL	SMC_EXTAL	46 47
		CLK_XTAL	XTAL	SMC_XTAL	46 47

SMC THERMAL NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
□	THERM DIF	THERMAL	SNS T1 DP1	52
□	THERM DIF	THERMAL	SNS T1 DN1	52
□	THERM DIF	THERMAL	SNS T1 DP2 DN3	44 52
□	THERM DIF	THERMAL	SNS T1 DN2 DP3	44 52
□	THERM DIF	THERMAL	SNS T2 DP1	52
□	THERM DIF	THERMAL	SNS T2 DN1	52
□	THERM DIF	THERMAL	SNS T2 DP2	52
□	THERM DIF	THERMAL	SNS T2 DN2	52
□	THERM DIF	THERMAL	SNS T2 DP3	52
□	THERM DIF	THERMAL	SNS T2 DN3	52
□				
□	THERM DIF	THERMAL	SNS ODD P	52 92
□	THERM DIF	THERMAL	SNS ODD N	52 92
□	THERM DIF	THERMAL	SNS CPU H P	52
□	THERM DIF	THERMAL	SNS CPU H N	52
□	THERM DIF	THERMAL	SNS SKIN P	52 92
□	THERM DIF	THERMAL	SNS SKIN N	52 92
□				
□	THERM DIF	THERMAL	SNS AMB P	52 54 92
□	THERM DIF	THERMAL	SNS AMB N	52 54 92
□	THERM DIF	THERMAL	SNS MXM P	52
□	THERM DIF	THERMAL	SNS MXM N	52
□				
□		THERMAL	HDD_OOB_TEMP_FILT	51 92
□		THERMAL	HDD_OOB_TEMP	51
□		THERMAL	HDD_OOB_TEMP_R	51
□		THERMAL	SMC_HDD_OOB_TEMP	46 51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	THERM_DIEF	THERMAL	SENSE MXM P	50
	THERM_DIEF	THERMAL	SENSE MXM N	50
	THERM_DIEF	THERMAL	SENSE VTT R P	
	THERM_DIEF	THERMAL	SENSE VTT R N	
	THERM_DIEF	THERMAL	SENSE CPU 1V5 P	50
	THERM_DIEF	THERMAL	SENSE CPU 1V5 N	50
	THERM_DIEF	THERMAL	SENSE CPU VTT P	
	THERM_DIEF	THERMAL	SENSE CPU VTT N	
		THERMAL	GND_SMC_AVSS	46 47 50
		THERMAL	SMC_CPU_1V5_ISENSE	46 50
		THERMAL	SMC_CPU_1V5_ISENSE_R	50
		THERMAL	SMC_CPU_1V5_VSENSE	46 50
		THERMAL	SMC_CPU_VSENSE	46 50
	VTD_PHY	VR_CTL	VR_CPU_IOUT	12 65
	THERM_DIEF	THERMAL	VR_ISNS_CPU_P	50
	THERM_DIEF	THERMAL	VR_ISNS_CPU_N	50
		THERMAL	SNS_PS_CPU_ISNS	50
		THERMAL	SMC_CPU_ISENSE	46 50

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8								7								6								5								4								3								2								1															
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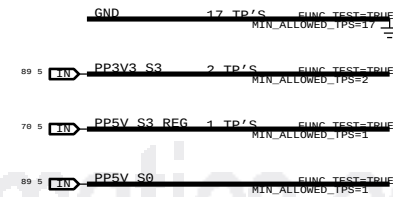
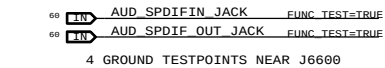
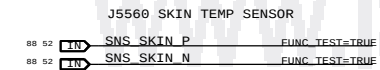
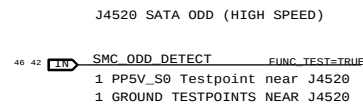
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PAGE TITLE					
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 Apple Inc.		DRAWING NUMBER	051-8337		
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PM NET PROPERTIES
(PM, RESET, EN, PG00D)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

NET_TYPE			
PHYSICAL	SPACING		
E17	PM	PLT RESET L	19 27
E14	PM_VTT	PLT RESET LS1V1 L	10
E14	PM	PM ACDC PS ON	5
E15	PM	PM BATLOW L	14 18 46
E16	PM	PM CLK32K SUSCLK	8 46 85
E16	PM	PM CLK32K SUSCLK_R	8 18 85
E16	PM	PM CLKRUN L	14 18 46 48
E16	PM	PM EXT TS L<0>	
E16	PM	PM EXT TS L<1>	
E19	PM	PM LAN PWRGD	14 18
E139	PM_VTT	FSB CPURSTOUT L	10 24
E16	PM_VTT	PM MEM PWRGD	10 18
E24	PM	PM ME PWRGD	18 64
E181	PM	PM MXM PG00D	64 75
E25	PM	PM PCH PWRGD	18 64
E183	PM	PM PG00D DDRREG S3	63 71
E183	PM	PM PG00D PVCORE CPU	25 64 65
E182	PM	PM PWRBTN L	18 24 46
E185	PM	PM RSMRST L	46 63
E185	PM	PM RSMRST_PCH L	18 63
E185	PM	PM SLP_M L	18 63
E183	PM	PM SLP_S3 L	5 18 26 36 46 47 63 64 81
E1820	PM	PM SLP_S4_1 L	18 63
E185	PM	PM SLP_S4 L	18 47
E143	PM	PM SLP_S5 L	18 47
E185	PM_VTT	PM SUS_PWR ACK	18
E185	PM	PM SYNC	10 18
E185	PM	SDCARD_PLT_RST L	27 44
E143	PM	PM SYSRST L	18 27 46
E143	PM	PM SYS_PWRGD	18 64
E143	PM_VTT	PM THRMTRIP L	10 20 47
E143	PM	RSMRST_PWRGD	46 64
E185	PM	RTC RESET L	17 91
E185	PM_VTT	CPU_PWRGD	10 20 24
E185	PM	CPU RESET L	10 27
E185	PM	PG00D_1V8_S0_G1	64
E185	PM	PG00D_1V8_S0_G2	64
E185	PM	PG00D_CPU_GFX_DDR	64
E185	PM	PG00D_P1V5_S0	10 73
E185	PM	PG00D_P1V8_S0	64
E185	PM	PG00D_P3V3_S0	64 73
E185	PM	PG00D_P3V3_S3	34 73
E185	PM	PG00D_P5V_S0	63 73
E185	PM	PG00D_PCH_AND_P1V8	64
E185	PM	PG00D_PCH_S0	64
E185	PM	PG00D_SYSPWR0K	64
E185	PM	PG00D_SYSPWR0K_R	64
E185	PM	RTC RESET L	17 91
E185	PM	P12V_S3_EN	
E185	PM	P1V5_S0_EN	63 73
E185	PM	P3V3S0_EN	63 73
E185	PM	P3V3S3_EN	63 73
E185	PM	P5VS0_EN	63 73
E185	PM	P5VS3_EN	63 70
E185	PM	PCHCORE_REG_EN	63 69
E185	PM	PCHCORE_REG_PG00D	63 64 69
E185	PM	PEG RESET L	8 27
E185	PM	SDCARD RESET	20 44 92

NET_TYPE			
PHYSICAL	SPACING		
E182	PM	4V5_REG_EN	56
E181	PM	ALL_SYS_PWRGD_R	5 64
E184	PM	ALL_SYS_PWRGD_SMC	46 64
E183	PM	CK505_27MHZ_EN	25
E185	PM	CPUVTT_REG_EN	63 68
E185	PM_VTT	CPUVTT_REG_PG00D	10 63 64 68
E187	PM	CPU_MEM_RESET_L	10 26
E188	PM	DDRVT EN	63 71
E188	PM	DEBUG_RESET_L	27 48
E190	PM	FWPHY_RESET_L	39
E191	PM	FWXIO_SNOOP_EN	39
E192	PM	FW_RESET_L	27 39
E195	PM	ENET_RESET_L	27 37
E197	PM	MEM_RESET_L	26 30 31
E196	PM	MINI_RESET_L	27 33
E198	PM	SMC_DELAYED_PWRGD	47 64
E110	PM	SMC_LRESET_L	27 46
E195	PM	SMC_RESET_L	46 47 48
E110	PM_VTT	XDP_CPUPWRGD	10 24
E110	PM_VTT	XDP_DBRESET_L	10 24 27
E110	PM_VTT	XDP_PWRGD	24



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